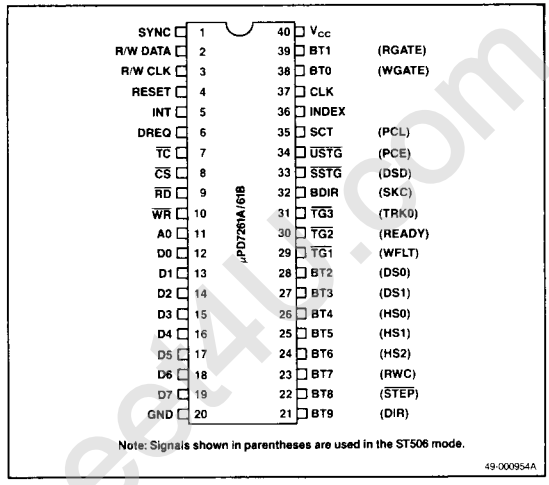
Description

The μPD7261A and μPD7261B hard-disk controllers are intelligent microprocessor peripherals designed to control a number of different types of disk drives. They are capable of supporting either hard-sector or soft-sector disks and provide all control signals that interface the controller with either SMD disk interfaces or ST506-type drives. The sophisticated instruction set minimizes the software overhead for the host microprocessor. By using the DMA controller, the microprocessor needs only to load a few command bytes into the μPD7261A/7261B and all the data transfers associated with read, write, or format operations are done by the μPD7261A/7261B and the DMA controller. Extensive error reporting, verify commands, ECC, and CRC data error checking assure reliable controller operation. The μPD7261A/7261B provides internal address mark detection, ID verification, and CRC or ECC checking and verification. An eight-byte FIFO is used for loading command parameters and obtaining command results. This makes the structuring of software drivers a simple task. The FIFO is also used for buffering data during DMA read/write operations.

Features

- ☐ Flexible interface to various types of hard disk drives
- ☐ Programmable track format
- ☐ Controls up to 8 drives in SMD mode; up to 4 drives in ST506-type mode
- ☐ Parallel seek operation capability
- ☐ Multi-sector and multi-track transfer capability
- ☐ Data scan and data verify capability
- ☐ High-level commands, including:
  Read Data, Read ID, Write Data, Format, Scan Data, Verify Data, Verify ID, Check, Seek (normal or buffered), Recalibrate (normal or buffered), Read Diagnostic (SMD only), Specify, Sense Interrupt Status, Sense Unit Status, and Detect Error
- ☐ NRZ or MFM data format
- ☐ Maximum R/W CLK frequency:
  — 12 MHz (7261A)
  — 18 MHz (7261B-18)
  — 23 MHz (7261B-23)
- ☐ Error detection and correction capability
- ☐ Simple I/O structure: compatible with most microprocessors
- ☐ All inputs and outputs except clock pins are TTL-compatible (clock pins require pullup)
- ☐ Data transfers under DMA control
- ☐ NMOS
- ☐ Single +5-volt power supply
- ☐ 40-pin ceramic DIP

Pin Configuration



Note: Signals shown in parentheses are used in the ST506 mode.

49-000954A

Ordering Information

Device Number	Package Type	Max Freq. of Operation
μPD7261AD	40-pin ceramic DIP	12 MHz
μPD7261BD-18	40-pin ceramic DIP	18 MHz
μPD7261BD-23	40-pin ceramic DIP	23 MHz

Pin Identification

No.	Symbol	Function
Host Interface		
4	RESET	Reset input
5	INT	Interrupt request output
6	DREQ	DMA request output
7	$\overline{TC}$	Terminal count input
8	$\overline{CS}$	Chip select input
9	$\overline{RD}$	Read strobe input
10	$\overline{WR}$	Write strobe input
11	A_0	Register select input
12–19	D_0–D_7	Data I/O bus
20	GND	Ground
37	CLOCK	External clock input
40	V_{CC}	+5 V power supply
SMD Interface		
1	SYNC	PLL synchronization output
2	R/W DATA	Read/write data I/O
3	R/W CLK	Read/write clock input

Pin Identification (cont)

No.	Symbol	Function
SMD Interface (cont)		
21-28, 38, 39	BT9-BT0	Bit 9-0 outputs / Status inputs
29-31	$\overline{TG1}$-$\overline{TG3}$	Tag 1-3 output
32	BDIR	Bit direction output
33	$\overline{SSTG}$	SR select tag output
34	$\overline{USTG}$	Unit select tag output
35	SCT	Sector input
36	INDEX	Sector zero input
ST506-Type Interface		
1	SYNC	PLL lock / Read clock enable output
2	R/W DATA	Read / write data I / O
3	R/W CLK	Read / write clock input
21	DIR	Direction in output
22	$\overline{STEP}$	Step pulse output
23	RWC	Reduced write current output
24-26	HS2-HS0	Head select outputs 2-0
27, 28	DS1, DS0	Drive select outputs 1, 0
29	WFLT	Write fault input
30	READY	Ready input
31	TRK0	Track zero input
32	SKC	Seek complete input
33	DSD	Drive selected input
34	PCE	Precomp early output
35	PCL	Precomp late output
36	INDEX	Index input
38	WGATE	Write gate output
39	RGATE	Read gate output

Pin Functions — Host Interface

RESET (Reset)

When the RESET input is pulled high, it forces the device into an idle state. The device remains idle until a command is issued to the system.

INT (Interrupt Request)

The μPD7261A/7261B pulls the INT output high to request an interrupt.

DREQ (DMA Request)

The μPD7261A/7261B pulls the DREQ output high to request a DMA transfer between the disk controller and the memory.

$\overline{TC}$ (Terminal Count)

The $\overline{TC}$ input goes low to signal the final DMA transfer.

$\overline{CS}$ (Chip Select)

When the $\overline{CS}$ input is low, it enables reading from or writing to the register selected by A_0.

$\overline{RD}$ (Read Strobe)

When the $\overline{RD}$ strobe is low, data is read from the selected register.

$\overline{WR}$ (Write Strobe)

When the $\overline{WR}$ input is low, data is written to the selected register.

A_0 (Register Select)

The A_0 input is connected to a non-multiplexed address bus line. When A_0 is high, it selects the command or status register. When it is low, it selects the data buffer.

D_0-D_7 (Data Bus)

D_0-D_7 are connected to the system data bus.

CLOCK (Clock)

The CLOCK input is the timing clock for the on-chip processor.

Pin Functions — SMD Interface

SYNC (PLL Synchronization)

This output goes high after the read gate signal (BT1 when $\overline{TG3} = 0$) is high and a given number of bytes (GPL2-2) has elapsed.

R/W DATA (Read/Write Data)

The R/W DATA pin outputs the write data to the drive, and inputs the read data from the drive.

R/W CLK (Read/Write Clock)

R/W CLK is the input for the read and write clocks.

BT9-BT0 (Bit 9-0)

BT9-BT0 output the bit signals, bit 9-0. The bit 9-0 outputs send cylinder and unit addresses to the drives. BT9-BT2 also act as inputs for status signals from the drives as shown in table 1.

Table 1. Bit and Control Information

No.	Bit	Control
21	BT9	Unit Selected
22	BT8	Seek End
23	BT7	Write Protected
24	BT6	
25	BT5	Unit Ready
26	BT4	On Cylinder
27	BT3	Seek Error
28	BT2	Fault

BT7-BT2 also read the device status 2 (SR7-SR2) and device type (DT7-DT2). The index and SCT pins read SR0, SR1 and DT0, DT1.

BDIR (Bit Direction)

The BDIR output determines whether pins 28-21 will output BT2-BT9 or input drive status signals.

$\overline{TG3}$-$\overline{TG1}$ (Tag 3-1)

The $\overline{TG}$ outputs define the use of the BT pins. When $\overline{TG1}$ is low, BT9-BT0 output the cylinder address. When $\overline{TG2}$ is low, BT7-BT0 select a head address. When $\overline{TG3}$ is low, BT9-BT0 output control signals for the disk drive.

$\overline{SSTG}$ (SR Select Tag)

When the $\overline{SSTG}$ output is low, BT7-BT2, INDEX and SCT will be inputting SR7-SR0 or DT7-DT0.

$\overline{USTG}$ (Unit Select Tag)

When the $\overline{USTG}$ output is low, BT4-BT2 will be outputting a unit address.

INDEX (Index)

The INDEX input goes high when the drive detects an index mark. INDEX also acts as the SR0 and DT0 input pin.

SCT (Sector)

The SCT input goes high when the drive detects a sector mark. SCT also acts as the SR1 and DT1 input pin.

Pin Functions — ST506-Type Interface

SYNC (Read Clock Enable)

SYNC indicates that a sync pattern has been detected and that synchronization has been achieved.

R/W DATA (Read/Write Data)

The R/W DATA pin outputs the write data to the drive, and inputs the read data from the drive.

R/W CLK (Read/Write Clock)

R/W CLK is the input for the read and write clocks.

DIR (Direction In)

The DIR output determines the direction the read/write head will move in when it receives a step pulse. DIR high will cause the head to move inward, DIR low will move the head outward.

$\overline{STEP}$ (Step Pulse)

$\overline{STEP}$ outputs the head step pulses.

RWC (Reduced Write Current)

The RWC output signals that the read/write head of the disk drive has selected a cylinder address larger than that specified in the SPECIFY command. This signal is used to reduce the write current.

HS2-HS0 (Head Select 2-0)

The HS2-HS0 outputs select the head. Up to 8 read/write heads can be selected per drive.

DS1, DS0 (Drive Select 1,0)

The DS1 and DS0 outputs select one of up to 4 drives.

WFLT (Write Fault)

The WFLT input detects write faults.

READY (Ready)

The READY input detects the drive's ready state.

TRK0 (Track 0)

The TRK0 input signals that the head is at track 0.

SKC (Seek Complete)

The SKC input signals that a seek is complete.

DSD (Drive Selected)

The DSD input signals that the drive is selected.

PCE (Precomp Early)

When the PCE output is high, early write precompensation is required.

PCL (Precomp Late)

When the PCL output is high, late write precompensation is required.

INDEX (Index)

The INDEX input goes high when the drive detects the index mark.

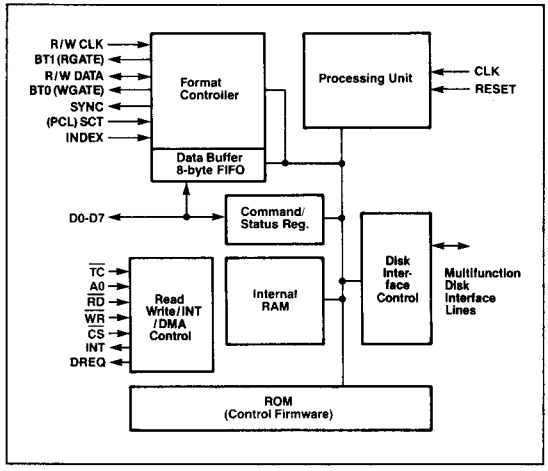
WGATE (Write Gate)

WGATE output goes high when the μPD7261A/7261B is writing data.

RGATE (Read Gate)

The RGATE output goes high when the μPD7261A/7261B is reading from the disk.

Block Diagram



Absolute Maximum Ratings

Operating temperature, T_{OPT}	0°C to +70°C
Storage temperature, T_{STG}	−65°C to +150°C
Voltage on any pin with respect to ground, V_{CC}	−0.5 to +7.0 V*
Input voltage, V_I	−0.5 to +7.0 V*
Output voltage, V_O	−0.5 to +7.0 V*

Comment: Exposing the device to stresses above those listed in the Absolute Maximum Ratings could cause permanent damage. The device should not be operated under conditions outside the limits described in the operational sections of this specification. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

*T_A = 25°C

DC Characteristics

*μPD7261B specifications are preliminary

T_A = 0 to +70°C, V_{CC} = +5.0 V ± 10% unless otherwise specified

Parameter	Symbol	Limits Min	Typ	Max	Unit	Test Conditions
Input voltage low	V_{IL1}	−0.5		+0.8	V	All except CLK, R/W CLK
Input voltage low	V_{IL2}	−0.5		+0.6	V	CLK, R/W CLK
Input voltage high	V_{IH1}	+2.0		V_{CC} +0.5	V	All except CLK, R/W CLK
Input voltage high	V_{IH2}	+3.3		V_{CC} +0.5	V	CLK, R/W CLK
Output voltage low	V_{OL}			+0.45	V	I_{OL} = +2.0 mA
Output voltage high	V_{OH1}	+2.4			V	I_{OH} = −100 μA, all except pins 21-34
Output voltage high	V_{OH2}	+2.4			V	I_{OH} = −50 μA, pins 21-34
Input leakage current	I_{LI1}			±10	μA	V_{IN} = V_{CC} to 0.45 V, all except pins 21-34
Input leakage current	I_{LI2}			−500 (7261A)	μA	V_{IN} = V_{CC} to 0.45 V; pins 21-34
				−700 (7261B)	μA	
Output leakage current	I_{LO}			±10	μA	V_{OUT} = V_{CC} to 0.45 V
Supply current	I_{CC}		250	320	mA	

Capacitance

T_A = 25°C, V_{CC} = 0 V

Parameter	Symbol	Limits Min	Typ	Max	Unit	Test Conditions
Input capacitance	C_{IN}			15	pF	(Note 1)
Output capacitance	C_{OUT}			15	pF	(Note 1)
Input/Output capacitance	$C_{I/O}$			20	pF	(Note 1)

Note:

(1) f = 1 MHz, All unmeasured pins tied to GND.

AC Characteristics

T_A = 0 to +70°C; V_{CC} = +5V ±10%; C_L = 100 pF (50 pF for 7261B-23)

Parameter	Symbol	Limits 7261A Min	7261A Max	7261B-18 Min	7261B-18 Max	7261B-23 Min	7261B-23 Max	Unit	Test Conditions
Processor Interface									
Clock cycle	t_{CY}	83		55		43		ns	
Clock time, low	t_{CL}	30		20		15		ns	
Clock time, high	t_{CH}	30		20		17		ns	
Clock rise time	t_{CR}		10		10		10	ns	
Clock fall time	t_{CF}		10		10		10	ns	
A_0, $\overline{CS}$ setup to $\overline{RD}$	t_{AR}	0		0		0		ns	
A_0, $\overline{CS}$ hold from $\overline{RD}$	t_{RA}	0		0		0		ns	
$\overline{RD}$ pulse width	t_{RR}	200		100		100		ns	
Data delay from $\overline{RD}$	t_{RD}		150		85		85	ns	
Output float delay	t_{RDF}	0	100	0	75	0	75	ns	
Data delay from A_0, $\overline{CS}$	t_{AD}		150		85		85	ns	
A_0, $\overline{CS}$ setup to $\overline{WR}$	t_{AW}	0		0		0		ns	
A_0, $\overline{CS}$ hold from $\overline{WR}$	t_{WA}	0		0		0		ns	
$\overline{WR}$ pulse width	t_{WW}	200		100		100		ns	
Data setup to $\overline{WR}$	t_{DW}	100		55		55		ns	
Data hold from $\overline{WR}$	t_{WD}	5		5		5		ns	
Recovery time from $\overline{RD}$, $\overline{WR}$	t_{RV}	200		70		70		ns	
Reset pulse width	t_{RES}	100		100		100		t_{CY}	
$\overline{TC}$ pulse width	t_{TC}	100		100		80		ns	
INT delay from $\overline{WR}$ ↑	t_{WI}		200		200		200	ns	
DREQ delay from $\overline{WR}$ ↑	t_{WRQ}		250		125		125	ns	
DREQ delay from $\overline{RD}$ ↑	t_{RRQ1}		250		160		160	ns	During disk read operation
DREQ delay from $\overline{RD}$ ↓	t_{RRQ2}		150		130		100	ns	After disk read operation
ST506-Type Interface									
R/W CLK cycle period	t_{RWCY}	83		83		83		ns	
R/W CLK time, low	t_{RWCL}	30		30		30		ns	
R/W CLK time, high	t_{RWCH}	30		30		30		ns	
R/W CLK rise time	t_{RWCR}		10		10		10	ns	
R/W CLK fall time	t_{RWCF}		10		10		10	ns	
R/W DATA setup to R/W CLK	t_{RDRC}	40		35		35		ns	
R/W DATA hold from R/W CLK	t_{RCRD}	5		5		5		ns	
R/W DATA delay from R/W CLK	t_{WCWD}	35	90	10	60	10	60	ns	
RGATE delay from R/W CLK	t_{RCRG}		300		300		300	ns	
WGATE delay from R/W CLK	t_{WCWG}		150		150		150	ns	
PCE / PCL delay from R/W CLK	t_{RWCPC}	35	110	10	80	10	80	ns	
SYNC delay from R/W CLK	t_{RWCSY}		150		150		150	ns	

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AC Characteristics (cont)

Parameter	Symbol	Limits 7261A Min	7261A Max	7261B-18 Min	7261B-18 Max	7261B-23 Min	7261B-23 Max	Unit	Test Conditions
ST506-Type Interface (cont)									
DS0, DS1 setup to $\overline{STEP}$	t_{DSST}	250		250		250		t_{CY}	Normal seek mode
DIR setup to $\overline{STEP}$	t_{DIST}	200		200		200		t_{CY}	
$\overline{STEP}$ pulse width	t_{STEP}	69	85	69	85	69	85	t_{CY}	
DS0, DS1 hold from $\overline{STEP}$	t_{STDS}	750		750		750		t_{CY}	Normal seek mode; polling mode
DIR hold from $\overline{STEP}$	t_{STDI}	750		750		750		t_{CY}	
DS0, DS1 hold from SKC	t_{SKDS}	100		100		100		t_{CY}	Normal seek mode; nonpolling
DIR hold from SKC	t_{SKDI}	100		100		100		t_{CY}	
DS0, DS1 setup to $\overline{STEP}$	t_{DSSTB}	250		250		250		t_{CY}	Buffered seek mode
DIR setup to $\overline{STEP}$	t_{DISTB}	200		200		200		t_{CY}	
$\overline{STEP}$ pulse width	t_{STEPB}	69	85	69	85	69	85	t_{CY}	
$\overline{STEP}$ cycle period	t_{STCY}	500	660	500	660	500	660	t_{CY}	
DS0, DS1 hold from $\overline{STEP}$	t_{STDSB}	200		200		200		t_{CY}	Buffered seek mode; polling mode
DIR hold from $\overline{STEP}$	t_{STDIB}	200		200		200		t_{CY}	
DS0, DS1 hold from SKC	t_{SKDSB}	100		100		100		t_{CY}	Buffered seek mode; nonpolling
DIR hold from SKC	t_{SKDIB}	100		100		100		t_{CY}	
Index pulse width	t_{IDXF}	8		8		8		t_{RWCY}	
SMD Interface									
R/W CLK cycle period	t_{RWCY}	83		55		43		ns	
R/W CLK time, low	t_{RWCL}	30		20		15		ns	
R/W CLK time, high	t_{RWCH}	30		20		17		ns	
R/W CLK rise time	t_{RWCR}		10		10		10	ns	
R/W CLK fall time	t_{RWCF}		10		10		10	ns	
R/W DATA setup to R/W CLK	t_{RDRC}	40		35		35	ns		
R/W DATA hold from R/W CLK	t_{RCRD}	5		5		5		ns	
R/W DATA delay from R/W CLK	t_{WCWD}	35	90	10	60	10	50	ns	
BT1 delay from R/W CLK	t_{RCRG}		300		300		300	ns	
BT0 delay from R/W CLK	t_{WCWG}		150		150		150	ns	
SYNC delay from R/W CLK	t_{RWCSY}		150		150		150	ns	
BDIR setup to $\overline{USTG}$	t_{BDUT}	60		60		60		t_{CY}	Unit select operation
BDIR hold from $\overline{USTG}$	t_{UTBD}	15		15		15		t_{CY}	
Unit ADR setup to $\overline{USTG}$	t_{UAUT}	38	52	38	52	38	52	t_{CY}	
Unit ADR hold from $\overline{USTG}$	t_{UTUA}	15		15		15		t_{CY}	
BDIR setup to $\overline{TG1}$	t_{BDT1}	27	48	27	48	27	48	t_{CY}	Cylinder select operation
BDIR hold from $\overline{TG1}$	t_{T1BD}	60		60		60		t_{CY}	

AC Characteristics (cont)

Parameter	Symbol	Limits 7261A Min	7261A Max	7261B-18 Min	7261B-18 Max	7261B-23 Min	7261B-23 Max	Unit	Test Conditions
SMD Interface (cont)									
CYL. ADR setup to $\overline{TG1}$	t_{CAT1}	27	48	27	48	27	48	t_{CY}	Cylinder select operation
CYL. ADR hold from $\overline{TG1}$	t_{T1CA}	24		24		24		t_{CY}	
$\overline{TG1}$ pulse width	t_{TG1}	24	36	24	36	24	36	t_{CY}	
BDIR setup to $\overline{TG2}$	t_{BDT2}	15		15		15		t_{CY}	Head select operation
BDIR hold from $\overline{TG2}$	t_{T2BD}	70		70		70		t_{CY}	
HEAD ADR setup $\overline{TG2}$	t_{HAT2}	15	70	15	70	15	70	t_{CY}	
HEAD ADR hold from $\overline{TG2}$	t_{T2HA}	24		24		24		t_{CY}	
$\overline{TG2}$, pulse width	t_{TG2}	24	36	24	36	24	36	t_{CY}	
BDIR setup to $\overline{TG3}$	t_{BDT3}	24		24		24		t_{CY}	RT2, FAULT CLR, SERVO, DATA STB control timing
BDIR hold from $\overline{TG3}$	t_{T3BD}	24	36	24	36	24	36	t_{CY}	
$\overline{TG3}$, pulse width	t_{TG3}	56	100	56	100	56	100	t_{CY}	
BT2, 3, 4, 6, 7, 8 setup to $\overline{TG3}$	t_{BTT3}		56		56		56	t_{CY}	
BT4, 6 hold from $\overline{TG3}$	t_{T3BT1}	24		24		24		t_{CY}	
BT2, 3, 7, 8 hold from $\overline{TG3}$	t_{T3BT2}	75		75		75		t_{CY}	
BDIR delay from $\overline{SSTG}$	t_{STBD}	24		24		24		t_{CY}	Sense unit status timing
BDIR high time	t_{BDIR}	54	66	54	66	54	66	t_{CY}	
BT9 setup to BDIR	t_{BTBD}	38	52	38	52	38	52	t_{CY}	
BT9 hold from BDIR	t_{BDBT}	24	33	24	33	24	33	t_{CY}	
$\overline{SSTG}$ pulse width	t_{SSTG}		370		370		370	t_{CY}	
Index pulse width	t_{IDXH}	8		8		8			
SCT pulse width	t_{SCT}	8		8		8			

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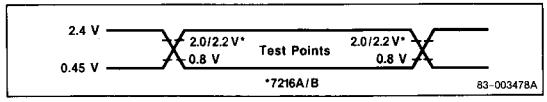
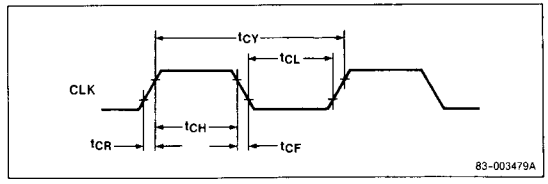
Timing Waveforms — Host System Interface

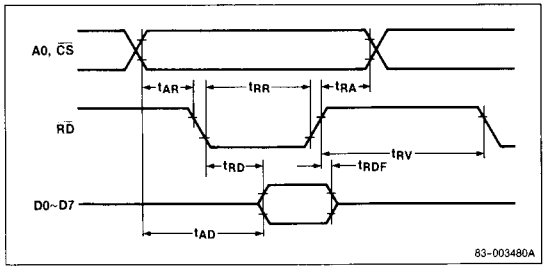
AC Test Points (Except R/W CLK, CLK)



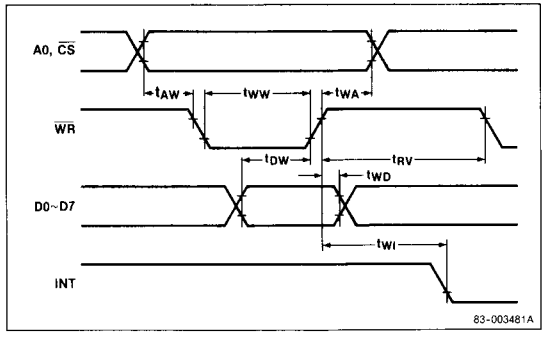
CLK Waveform



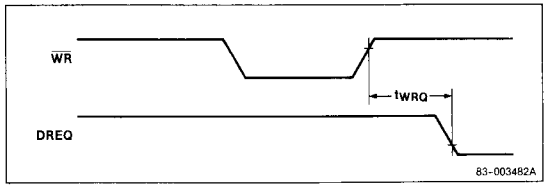
Read Timing



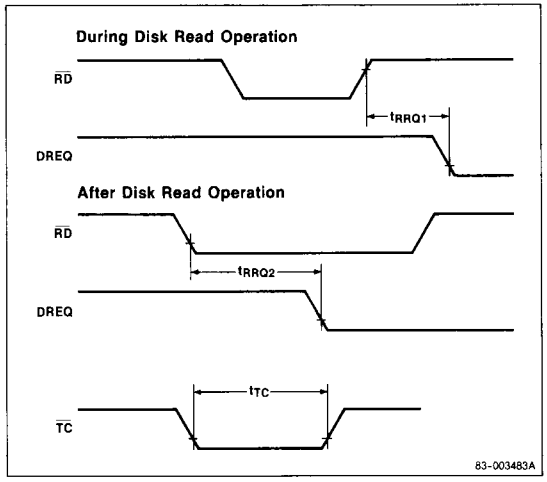
Write Timing



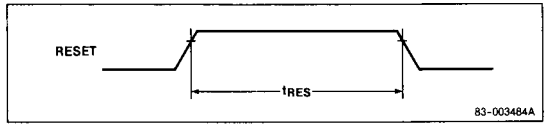
DMA Write Timing



DMA Read Timing

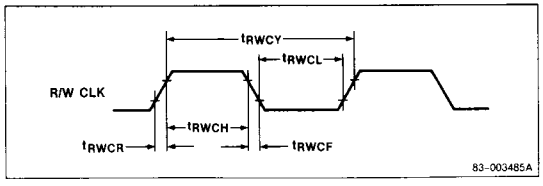


Reset Waveform

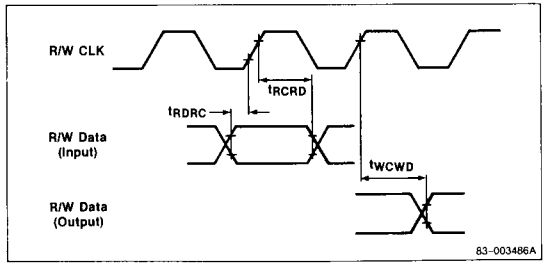


Timing Waveforms — SMD Interface

R/W CLK Waveform

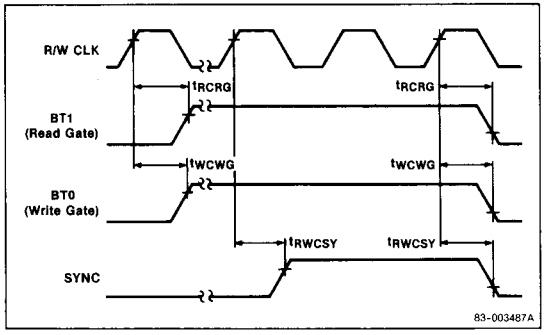


Data Read/Write Timing

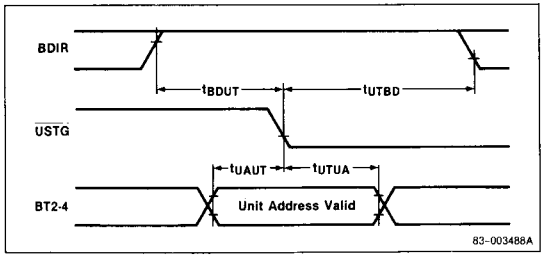


Timing Waveforms—SMD Interface (cont)

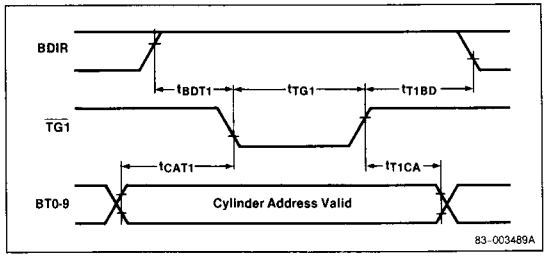
Read/Write Timing



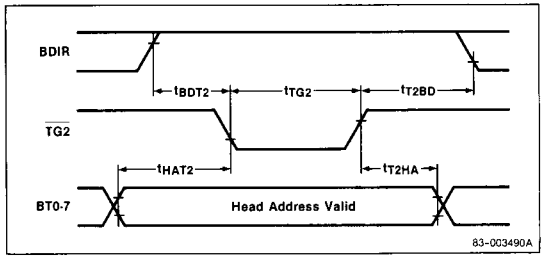
Unit Select Timing



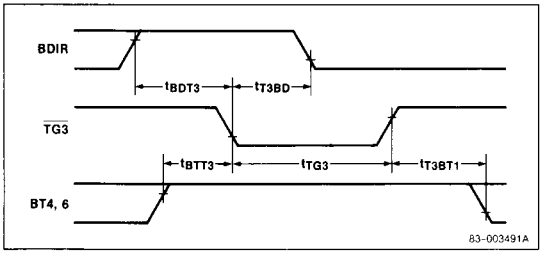
Seek Timing



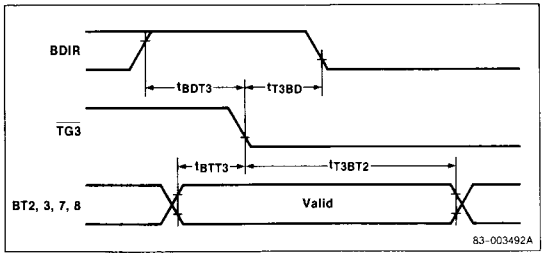
Head Select Timing



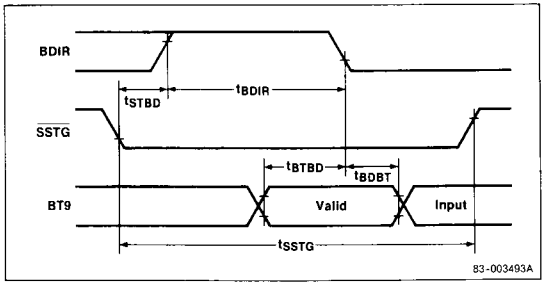
Bit Bus Timing, Fault Clear/Return-to-Zero



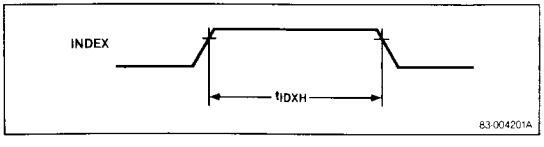
Bit Bus Timing, Servo Offset/Data Strobe



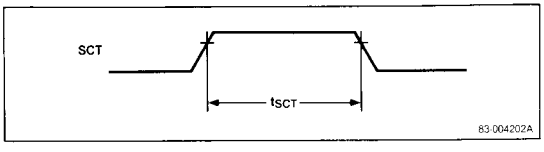
Bit Bus 9 Timing



Index Waveform



Sector Waveform



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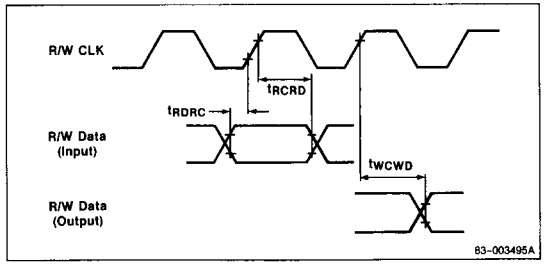
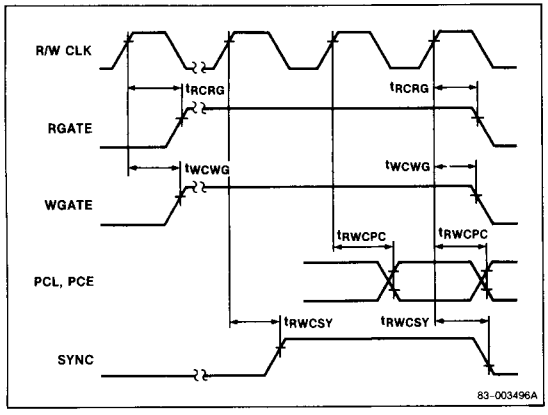
Timing Waveforms—ST506-Type Interface

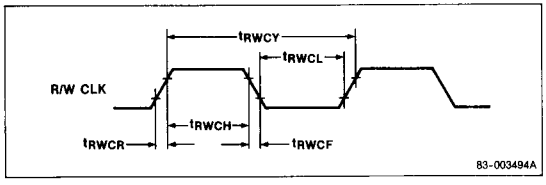
Data Read/Write Operation



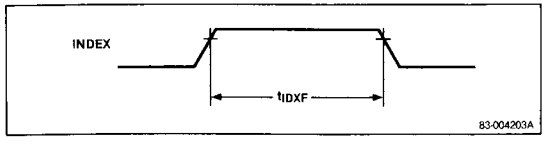
Read/Write Operation



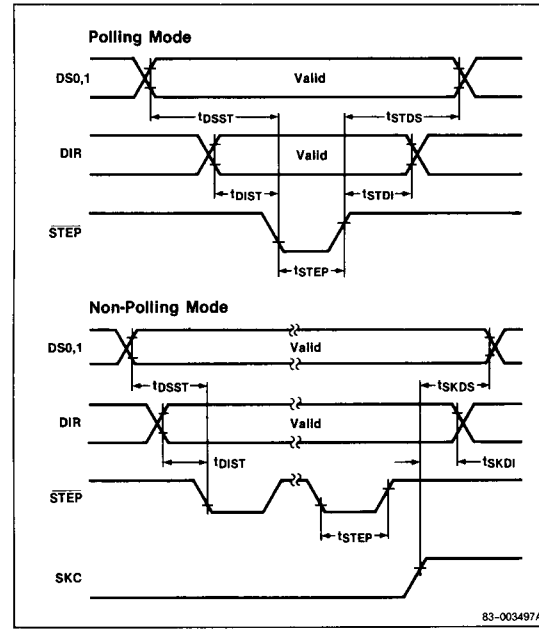
R/W CLK Waveform



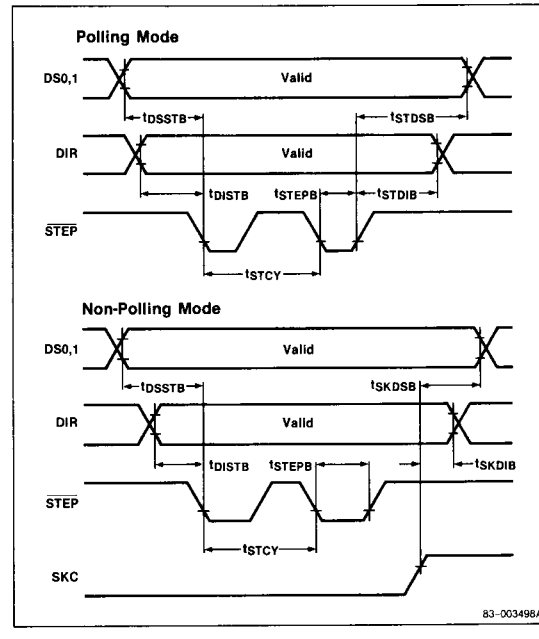
Index Waveform



Normal Seek Operation

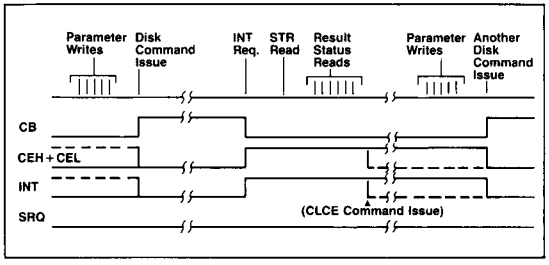


Buffered Seek Operation

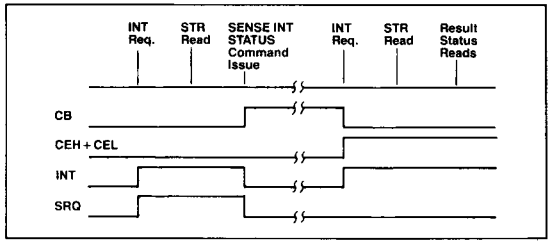


Timing Waveforms—ST506-Type Interface (cont)

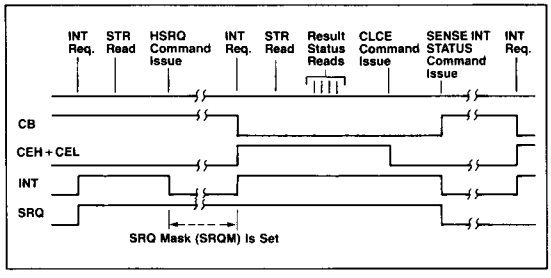
Read/Write Sequence (Disk Command Issue)



Sense Interrupt Status Request When Controller Not Busy



Sense Interrupt Status Request When Controller Busy



High-Level Commands

Specify

Allows user to select SMD or ST506-type mode data block length, ending track number, end sector number, gap length, track at which write current is reduced, ECC or CRC function, choice of polynomial, and polling mode enable.

Sense Interrupt Status

When a change of disk status occurs, the HDC will interrupt the host CPU. This command will reveal the cause of interrupt, such as seek end, disk ready change, seek error, or equipment check. The disk unit address is also supplied.

Sense Unit Status

The host CPU specifies the drive numbers and the HDC will return information such as write fault, ready, track 000, seek complete and drive selected, or for SMD units fault, seek error, on cylinder, unit ready, AM found, write protected, seek end, and unit selected.

Detect Error

Used after a read operation where ECC has been employed. The detect error command supplies the information needed to allow the host CPU to execute an error correction routine. (Only allowed when an actual correctable error is detected by the HDC.)

Recalibrate

Returns the disk drive heads to the home position or track 000 position. Has four modes of operation: SMD, normal, buffered, or nonpolling.

6

Seek

Moves the disk drive heads to the specified cylinder. As in recalibrate, seek has four modes of operation.

Format

This command is used to initialize the medium with the desired format which includes various gap lengths, data patterns, and CRC codes. This command is used in conjunction with the specify command.

Verify ID

Used to verify the ID bytes with data from memory. Performs the operation over a specified number of sectors.

Read ID

Used to verify the position of the read/write heads.

Read Diagnostic

Used in SMD mode only, the command allows the programmer to read a sector of data even if the ID portion of the sector is defective. Only one sector at a time can be read.

Read Data

Reads and transfers to the system memory the number of sectors specified. The HDC can read multiple sectors and multiple tracks with one instruction.

Scan

Compares a specified block of memory with specified sectors on the disk. The 7261A/7261B continues until a sector with matching data is found, until the sector count reaches zero, or the end of the cylinder is reached.

Verify Data

Makes a sector-by-sector comparison of data in the system memory by DMA transfer. As in read operation, multiple sectors and tracks may be verified with this commmand.

Write Data

Data from the system memory, transferred by DMA, is written onto the specified disk unit. As in the read command, data may be written onto successive sectors and tracks.

Auxiliary Command

Allows four additional functions to be executed: software reset, clear data buffer, mask interrupt request bit (masks interrupts caused by change of status of drives), and reset interrupt caused by command termination (used when no further disk commands will be issued, which would normally reset the interrupt).

Command Operation

There are three phases for most of the instructions that the μPD7261A/7261B can execute: command phase, execution phase, and result phase. During the command phase the host CPU loads preset parameters into the μPD7261A/7261B FIFO via the data bus and by successive write pulses to the part with A_0 and CS true low. Once the required parameter bytes are loaded the appropriate command is initiated by issuing a write pulse with A_0 high and CS low and the command code on the data bus.

The μPD7261A/7261B is now in the execution phase. This can be verified by examining the status register bit 7 (the controller busy bit). The execution phase is ended when a normal termination or an abnormal termination occurs. An abnormal termination can occur due to a read or write error, or a change of status in the addressed disk drive. A normal termination occurs when the command given is correctly completed. (This is indicated by bits in the status register.) The result phase is then entered. The host CPU may read various result parameters from the FIFO. These result parameters may be useful in determining the cause of an interrupt, or the location of a sector causing a read error, for example.

The chart shown in table 2 illustrates the preset parameters and result parameters that are associated with each command. The abbreviations are defined at the end of table 2.

Table 2. Preset Parameters and Result Status Byte

Disk Command	Command Code	Preset Parameters/Result Status 1st	2nd	3rd	4th	5th	6th	7th	8th
Detect error	0100X								
		EADH	EADL	EPT1	EPT2	EPT3			
Recalibrate	0101[B]								
		IST*							
Seek	0110[B]	PCNH	PCNL						
		IST*							
Format	0111(S)	PHN	(PSN)	SCNT	DPAT	GPL1	[GPL3]		
		EST	SCNT						
Verify iD	1000(S)	PHN	(PSN)	SCNT					
		EST	SCNT						
Read ID	1001(S)	PHN	(PSN)	SCNT					
		EST	SCNT						
(Read diagnostic)	1010X	PHN	PSN						
		EST							
Read data	1011X	PHN	(FLAG)	LCNH	LCNL	LHN	LSN	SCNT	
		EST	PHN	(FLAG)	LCNH	LCNL	LHN	LSN	SCNT
Check	1100X	PHN	(FLAG)	LCNH	LCNL	LHN	LSN	SCNT	
		EST	PHN	(FLAG)	LCNH	LCNL	LHN	LSN	SCNT
Scan	1101X	PHN	(FLAG)	LCNH	LCNL	LHN	LSN	SCNT	
		EST	PHN	(FLAG)	LCNH	LCNL	LHN	LSN	SCNT
Verify data	1110X	PHN	(FLAG)	LCNH	LCNL	LHN	LSN	SCNT	
		EST	PHN	(FLAG)	LCNH	LCNL	LHN	LSN	SCNT
Write data	1111X	PHN	(FLAG)	LCNH	LCNL	LHN	LSN	SCNT	
		EST	PHN	(FLAG)	LCNH	LCNL	LHN	LSN	SCNT
Sense interrupt status	0001X	IST							
Specify	0010X	MODE	DTLH	DTLL	ETN	ESN	GPL2	(MGPL1) [RWCH]	[RWCL]
Sense unit status	0011X								
		UST							

Note:
( ): These are omitted for soft-sector disks.
[ ]: These are omitted for hard-sector disks.
*: IST available as a result byte only when in nonpolling mode.
B: Indicates buffered mode when set.
S: Indicates Skewed mode (SMD only) when set.
X: Indicates don't care.

Mnemonic Definitions

EADH Error address, high byte
EADL Error address, low byte
EPT1 Error pattern, byte one
EPT2 Error pattern, byte two
EPT3 Error pattern, byte three
PCNH Physical cylinder number, high byte

Mnemonic Definitions (cont)

PCNL Physical cylinder number, low byte
PHN Physical head number
PSN Physical sector number
SCNT Sector count
DPAT Data pattern
GPL1 Gap length one
GPL3 Gap length three
EST Error status byte
FLAG Flag byte
LCNH Logical cylinder number, high byte

Mnemonic Definitions (cont)

LCNL	Logical cylinder number, low byte
LHN	Logical head number
LSN	Logical sector number
IST	Interrupt status byte
MODE	Mode
DTLH	Data length, high byte
DTLL	Data length, low byte
ETN	Ending track number
ESN	Ending sector number
GPL2	Gap length two
RWCL	Write current cylinder, low byte
RWCH	Write current cylinder, high byte
UST	Unit status byte
MGPL1	Modified gap length 1

Status Register

This register is a read only register and may be read by asserting $\overline{RD}$ and $\overline{CS}$ with A_0 high. The status register may be read at any time. It is used to determine controller status and partial result status. See table 3.

Table 3. Status Register Bits

Pin No.	Pin Name	Function
D_7	CB (Controller busy)	Set by a disk command issue. Cleared when the command is completed. (This bit is also set by an external reset signal or an RST command, but will be cleared at the completion of the reset function.) When this bit is set, a new disk command will not be accepted.
D_6, D_5	CEH, CEL (Command end)	CEH = 0 and CEL = 0 A disk command is in process, or no disk command is issued after the last reset signal or the last CLCE auxiliary command. Both the CEH and CEL bits are cleared by a disk command, a CLCE auxiliary command, or a reset signal.
		CEH = 0 and CEL = 1 Abnormal termination of a disk command. Execution of a disk command was started, but was not successfully completed.
		CEH = 1 and CEL = 0 Normal termination of a disk command. The execution of a disk command was completed and properly executed.
		CEH = 1 and CEL = 1 Invalid command issue.

Table 3. Status Register Bits (cont)

Pin No.	Pin Name	Function
D_4	SRQ (Sense interrupt status request)	When a seek end, an equipment check condition, or a ready signal state change is detected, this bit is set requesting a sense interrupt status command be issued to take the detailed information. This bit is cleared by an issue of that command or by a reset signal.
D_3	RRQ (Reset request)	Set when controller has lost control of the format controller (missing address mark, for example). An auxiliary RST command or RESET signal will clear this bit.
D_2	IER (ID error)	Set when a CRC error is detected in the ID field. An auxiliary RST or another disk command will reset this bit.
D_1	NCI (Not coincident)	Set if the controller cannot find a sector on the cylinder which meets the comparison condition during the execution of a scan command. This bit is also set if data from the disk does not coincide with the data from the system during a verify ID or a verify data command. This bit is cleared by a disk command or a reset signal.
D_0	DRQ (Data request)	During execution of write ID, verify ID, scan, verify data, or a write data command, this bit is set to request that data be written into the data buffer. During execution of read ID, read diagnostic, or read data command, this bit is set to request that data be read from the data buffer.

Error Status Byte

This byte is available to the host at the termination of a read, write, or data verification command and provides additional error information to the host CPU. If the status register indicates a normal command termination, it can be assumed that the command was executed without error and it is not necessary to read this byte. When it is necessary to determine the cause of an error this byte may be read by issuing an $\overline{RD}$ pulse with $\overline{CS}$ and A_0 low. The remaining result bytes associated with a particular command may be read by issuing additional $\overline{RD}$ pulses. Data transfer from or to the FIFO is asynchronous and may occur at rates up to 2.5 Mbytes per second. See table 4.

Table 4. Error Status Bits

Pin No.	Pin Name	Function
D_7	ENC (End of cylinder)	Set when the controller tries to access a sector beyond the final sector of a cylinder. Cleared by a disk command or an auxiliary RST command.
D_6	OVR (Overrun)	When set, indicates that the FIFO became full during a read operation, or empty during a write operation.
D_5	DER (Data error)	A CRC or an ECC error was detected in the data field.
D_4	EQC (Equipment check)	A fault signal from the drive has been detected or a track 0 signal has not been returned within a certain time interval after the recalibrate command was issued.
D_3	NR (Not ready)	The drive is not in ready state.
D_2	ND (No data)	The sector specified by ID parameters was not found on the track.
D_1	NWR (Not writable)	Set if write protect signal is detected when the controller tries to write on the disk. It is cleared by a disk command or by an auxiliary RST command.
D_0	MAM (Missing address mark)	This bit is set if during execution of read data, check, scan, or verify data commands, no address mark was found in the data field or if during execution of a read ID or verify ID command, no address mark was detected in the ID field.

Interrupt Status Byte

This byte is made available to the host CPU by executing the Sense Interrupt Status command. This command should be issued only when the μPD7261A/7261B requests it, as indicated by bit D_4 of the status register. This byte reveals changes in disk drive status that have occurred. See table 5.

Table 5. Interrupt Status Bits

Pin No.	Pin Name	Function
D_7	SEN (Seek end)	A seek end or seek complete signal has been returned after a seek or a recalibrate command was issued.
D_6	RC (Ready change)	The state of the ready signal from the drives has changed. The state itself is indicated by the NR bit.
D_5	SER (Seek error)	Seek error has been detected on seek end.
D_4	EQC (Equipment check)	Identical to bit 4 of the error status byte.
D_3	NR (Not ready)	Identical to bit 3 of the error status byte.
D_2–D_0	UA_2–UA_0 (Unit address)	The unit address of the drive which caused an interrupt request on any of the above conditions.

Drive Interface

The μPD7261A/7261B has been designed to implement two of the more popular types of interfaces: the SMD (Storage Module Drive) and the floppy-like Winchester drive which has come to be known as the ST506 interface. The desired interface mode is selected by the Specify command.

ST506-Type Interface

In the ST506 mode the μPD7261A/7261B performs MFM encoding and decoding at data rates to 6 MHz and provides all necessary drive interface signals. Included internally is circuitry for address mark detection, sync area recognition, serial-to-parallel-to-serial conversion, an 8-byte FIFO for data buffering, and circuitry for logical addressing of the drives. External circuitry required consists of control signal buffering, a delay network for precompensation, a phase-lock loop, a write clock oscillator and a differential transceiver for drive data. The floppy-like interface can be implemented with as few as 7 IC's using NEC's hard-disk interface chip, the μPD9306A, or with 12 to 14 SSI ICs. See figure 1.

Figure 1. μPD7261A/7261B ST506-Type Interface

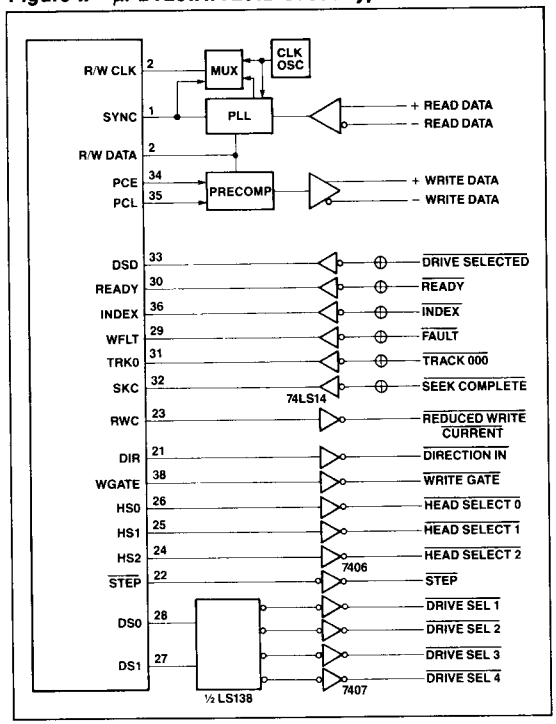
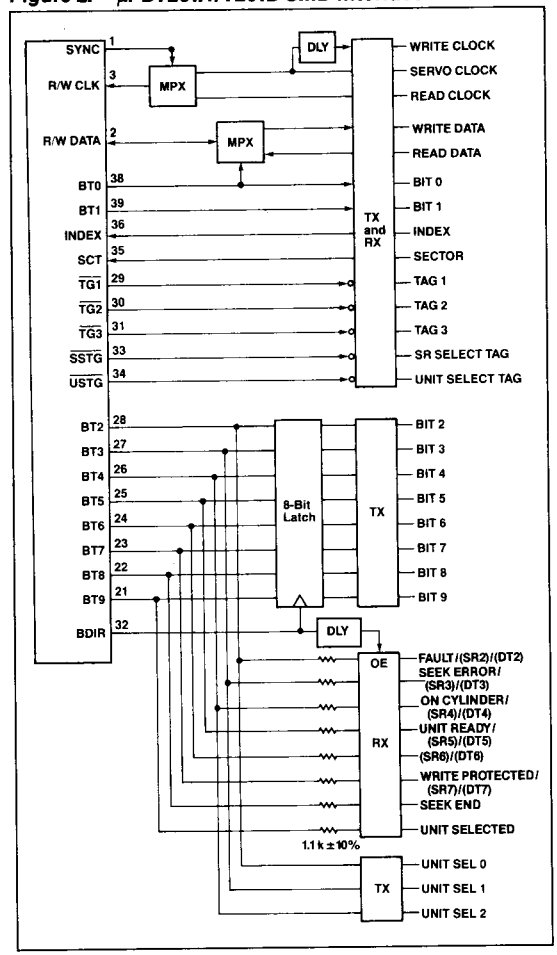


Figure 2. μPD7261A/7261B SMD Interface



SMD Interface

In the SMD mode the μPD7261A/7261B will support data rates to 10 MHz/15 MHz in the NRZ format. All control functions necessary for an SMD interface are implemented on-chip with de-multiplexing of 8 data lines performed externally by a single 8-bit latch. A small amount of logic is required to multiplex the data and clock lines, and differential drivers and receivers are required to implement the actual interface. Depending on individual logic design and the number of drives used, the SMD interface may be implemented with as few as 12 ICs. See figure 2.

Note:
CLK (pin 37) frequency must be a minimum of 1.1 × NRZ data rate.

Internal Architecture

The μPD7261A/7261B can be divided into three major internal logic blocks: command processor; format controller; microprocessor interface.

Command Processor

The command processor is an 8-bit microprocessor with its own instruction set, program ROM, scratchpad RAM, ALU, and I/O interface. Its major functions are:

- ☐ To decode the commands from the host microcomputer that are received through the 8-bit data bus
- ☐ To execute seek and recalibrate commands
- ☐ To interface to the drives and read the drive status lines
- ☐ To load the format controller with the appropriate microcode, enabling it to execute the various read/write data commands.

The command processor microprocessor is idle until it receives the command from the host microcomputer. It then reads the parameter bytes from the FIFO, and loads them into its RAM. The command byte is decoded and, depending on its opcode, the appropriate subroutine from the 2.6K internal ROM is selected and executed. Some of these commands are executed by the command processor without involvement of the format

controller. When data transfers to and from the disk are made, the command processor loads the appropriate microcode into the format controller, then relinquishes control. When the data transfer is complete, the command processor again takes control. One other important function that the command processor performs is managing the interface to the disk drives. The command processor contains an I/O port structure similar to many single-chip microcomputers in that the ports may be configured as input or output pins. Depending on the mode of operation selected by the Specify command, the command processor will use the bidirectional I/O lines for different functions.

Command Register

This register is a write only register. It is selected when the A_0 input is high and the $\overline{CS}$ input is low. There are two kinds of commands: disk commands and auxiliary commands. Each command format is shown in figure 3.

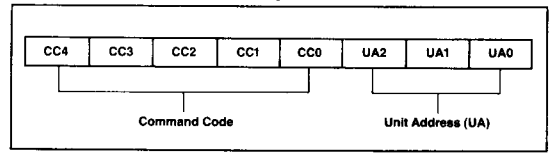
An auxiliary command is accepted at any time and is immediately executed, while a disk command is ignored if the on-chip processor is busy processing another disk command. A valid disk command causes the processor to begin execution using the parameters previously loaded into the data buffer. Disk commands and the parameters needed are described in the Microprocessor Interface section.

Command Codes

CC4	CC3	CC2	CC1	CC0		
0	0	0	0	X		(Auxiliary Command)
0	0	0	1	X		Sense int. status (Note 1)
0	0	1	0	X		Specify (Note 1)
0	0	1	1	X		Sense unit status
0	1	0	0	X		Detect error (Note 1)
0	1	0	1	[B]		Recalibrate
0	1	1	0	[B]		Seek
0	1	1	1	[S]		Format
1	0	0	0	[S]		Verify ID
1	0	0	1	[S]		Read ID
1	0	1	0	X		Read diagnostic
1	0	1	1	X		Read data
1	1	0	0	X		Check
1	1	0	1	X		Scan
1	1	1	0	X		Verify data
1	1	1	1	X		Write data

Note:
(1) The UA field is 000.
[B] Indicates buffered mode when set.
[S] Indicates skewed mode when set.

Figure 3. Disk Command Byte



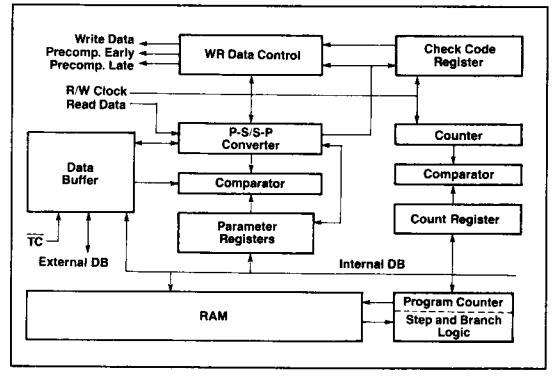
Format Controller

The format controller is built with logic that enables it to execute instructions at very high speed: one instruction per single clock cycle. The major functions it performs are:

- Serial-to-parallel and parallel-to-serial data conversion
- CRC and ECC generation and checking
- MFM data decoding and encoding
- Write precompensation
- Address mark detection and generation
- ID field search in soft-sector format
- DMA data transfer control during read/write operations.

The major blocks in the format controller are the sequencer and the serial/parallel data handler. The sequencer consists of a writable control store (32 words by 16 bits), a program counter, branch logic, and the parameter register. The serial/parallel logic consists of a parallel-to-serial converter for disk write operations, a serial-to-parallel converter for disk read operations, precompensation logic for writing MFM data, comparator logic that locates sync fields, address marks, and ID fields. There is also comparator logic that is used during Verify Data commands. See figure 4.

Figure 4. Block Diagram of the Format Controller



6

Microprocessor Interface

Read/Write Control. The internal registers are selected as shown in truth table 6.

Table 6. Register Selection Table

$\overline{CS}$	A_0	$\overline{RD}$	$\overline{WR}$	Selection
0	0	0	1	Data buffer register (Note 1)
0	0	1	0	Data buffer register (Note 1)
0	1	0	1	Status register
0	1	1	0	Command register
0	X	1	1	Don't care
1	X	X	X	Don't care
0	X	0	0	Inhibited

Note:
(1) Preset parameters and result status information are written and read from the result status register in the HDC through this data buffer register.

Interrupt. The interrupt request line is activated or inactivated according to the following equation:

$$INT = CEH + CEL + SRQ \bullet \overline{SRQM}$$

This means that if either of the command end bits is set or if the sense interrupt status request bit is set (and the SRQM mask is not set), then an interrupt will be generated. The command end bits, CEH and CEL, are set by command termination.

The SRQ bit is set when an equipment check condition or a state change of the ready signal from the disk drives is detected. It is also set when a seek operation is completed. Under these conditions the INT line is activated unless the SRQM mask is set.

Both of the CEH and CEL bits are cleared by a disk command, but both bits may be cleared before the next disk command by issuing a CLCE auxiliary command.

The interrupt caused by the SRQ bit indicates that a sense interrupt status command should be issued by the host microprocessor so that it can determine the exact cause of the interrupt. However, the μPD7261A/7261B may be processing a disk command when the interrupt occurs. Since it is not possible to issue a disk command while the μPD7261A/7261B is busy, an HSRQ auxiliary command can be issued to set the SRQM (sense interrupt request mask) and mask the interrupt. The SRQM is reset upon completion of the disk command in progress.

DMA Control. When true, the DREQ pin and the DRQ (data request) bit of the status register indicate a request for data transfer between the disk controller and external memory. These are activated during execution of the following disk commands:

HDC ← memory: Format, Verify ID, Scan, Verify Data, Write Data

HDC → memory: Read ID, Read Diagnostic, Read Data

Data being read from a disk or external memory is temporarily stored in the data buffer (8 bytes maximum), and is transferred to external memory or a disk, respectively.

Data transfers are terminated externally by a reset signal or by a read or a write data operation coinciding with an active terminal count ($\overline{TC}$) signal. They are also terminated internally when an abnormal condition is detected or all the data specified by the sector count parameter (SCNT) has been transferred.

Data transfers are accomplished by $\overline{RD}$ or $\overline{WR}$ signals to the μPD7261A/7261B when DREQ is active. During read operations, DREQ goes active when the FIFO contains three or more bytes. If the FIFO contains three bytes and an $\overline{RD}$ pulse is issued, DREQ goes low within t_{RRQ1}. DREQ will stay active on the final sector until the final byte is extracted. In this case, DREQ goes low within t_{RRQ2}. During write operations DREQ is asserted as soon as a Write Data command is accepted. DREQ remains high until the FIFO contains six bytes, at which time it goes low within t_{WAI}. DREQ corresponds to FIFO almost-full and FIFO almost-empty as implemented in the μPD7261A/7261B. This has been done so that a fast DMA controller may actually overrun the FIFO by one or two bytes without harm.

Commands

Recalibrate

0101B	
	IST*

The read/write heads of the specified drive are retracted to the cylinder 0 position. IST is available as a result byte only if polling mode is disabled. See Specify.

Hard-Sector. An RTZ (Return to Zero) signal is asserted on the bit-6 line with the TAG-3 bit being set. Then the CEH bit of the status register is set indicating a normal termination of the command.

After this command is given, the HDC checks the seek end, unit ready, and fault lines of the drive continually until an active signal is detected on these lines. Then the SRQ bit of the status register is set indicating that a sense interrupt status command should be performed. Each bit of the IST (interrupt status) byte is set according to the result, in anticipation of the sense interrupt status command.

Soft-Sector. There are four different ways to implement the Recalibrate command when the ST506 interface mode has been specified. Both polling and nonpolling modes of operation are provided, with both normal or buffered Recalibrate commands available in either mode.

Normal Mode with Polling. The CEH bit of EST is set to 1 immediately after the Recalibrate command is issued (a Recalibrate command may now be issued to another drive). The HDC now begins generating step pulses at the specified rate. The PCN for the drive is cleared and the TRK0 signal is checked while stepping pulses are sent to one or more drives. When TRK0 is asserted, the SEN (seek end) bit of the IST (interrupt status) byte is set and the SRQ bit of the status register is set. This causes an interrupt and requests that a sense interrupt status command be issued. If 1023 pulses have been sent and TRK0 is not asserted, then the SRQ bit is again set, but with the SER (seek error) and EQC (equipment check) bits of the IST byte set. The ready signal of each drive is checked before each step pulse is sent, and the Recalibrate command is terminated if the drive enters a not-ready state, whereby the NR bit of the IST byte is set to 1.

Normal Mode with Polling Disabled. Operation is similar to that in "Normal Mode with Polling", but the CEH and CEL bits of the status register are not set until either the SEN (seek end) or the SER (seek error) condition occurs. The SRQ bit is not set when polling is disabled, and the IST byte is now available as a result byte when the Recalibrate command is terminated (see "Preset Parameters and Result Status Bytes"). It is not possible to overlap Recalibrate operations in this mode.

Buffered Mode with Polling. This mode operates in a manner similar to that described as "Normal Mode with Polling", but with the following differences:

(1) 1023 step pulses are sent at a high rate of speed (approximately 50 μs between pulses)

(2) After the required number of pulses are sent, the CEH bit is set, and then additional Recalibrate or Seek commands will be accepted for other drives

(3) The SRQ bit is set when the drive asserts SKC, which causes the SEN bit of the IST byte to be set

(4) If SEN is not set within the time it takes to send 1023 "normal" pulses (i.e., when in normal stepping mode), then SER and EQC of the IST byte are set.

Buffered Mode with Polling Disabled. 1023 stepping pulses are immediately sent after the Recalibrate command is issued. CEH and/or CEL is set when SEN or SER occurs. SEN is set when TRK0 from the addressed drive is asserted. SER is set if TRK0 is not asserted within the time required to send 1023 "normal" pulses. The Recalibrate command will be terminated abnormally if a not-ready condition occurs prior to SEN being set. The SRQ bit of the status register is not set. The IST byte (interrupt status) is available as a result byte when either CEH or CEL is set.

Seek

0110B	PCNH	PCNL
	IST*	

PCNH = Physical Cylinder Number, High Byte
PCNL = Physical Cylinder Number, Low Byte

The read/write heads of the specified drive are moved to the cylinder specified by PCNH and PCNL. IST is available as a result byte only if polling mode is disabled. See Specify.

Hard-Sector. The contents of PCNH and PCNL are asserted on the BIT0 through BIT9 output lines of the SMD interface with the TAG1 control line being set. (The most significant six bits of PCNH are not used.) The CEH bit of the status register is then set, and the command is terminated normally.

The HDC then checks the seek end, unit ready and fault lines of the drive continually until an active signal is detected on these lines. The SRQ bit of the status register is then set requesting that a Sense Interrupt Status command be performed. Each bit of the IST (interrupt status) byte is set appropriately in anticipation of the Sense Interrupt Status command.

Soft-Sector (Normal Stepping, Polling Enabled). In this mode, the CEH bit of the status register is set to 1 as soon as the Seek command is issued. This allows a Seek or Recalibrate command to be issued to another drive. The HDC now sends stepping pulses at the specified rate and monitors the ready signal. Should the drive enter a not-ready state, the SER bit of the IST byte is set and the SRQ bit of the status register is set, causing an interrupt and requesting a Sense Interrupt Status command. When the drive asserts the seek complete (SKC) signal, the SEN bit of the IST byte is set and the SRQ bit of the status register is set, again requesting service.

Soft-Sector (Normal Stepping, Polling Disabled). Stepping pulses to the drive begin as soon as the Seek command is accepted. The ready signal is checked prior to each step pulse. If the drive enters a not-ready state the seek command is terminated abnormally (CEL = 1), and SER of the IST byte is set. If the seek operation is successful, the seek command will be terminated normally (CEH = 1) when the drive asserts SKC (seek complete). The SEN (seek end) bit of the IST byte is set and the IST (interrupt status) byte is available as a result byte. The Sense Interrupt Status command is not allowed (SRQ is not set), nor can seek operations be overlapped in this mode.

Soft-Sector (Buffered Stepping, Polling Enabled). As soon as the Seek command is accepted by the HDC, high-speed stepping pulses are generated. As soon as the required number of pulses are sent, CEH is set to 1, indicating a normal termination. Another Seek command in the same mode may now be issued. The drive is now controlling its own head positioner and asserts SKC when the target cyclinder is reached.) If the drive has not asserted SKC (seek complete) within the time it takes to send the required number of pulses in normal stepping mode, or if the drive enters a not-ready state, then the SER bit of the IST byte and the SRQ bit of the status register are set. Otherwise, the SEN bit of the IST byte is set, along with SRQ of the status register.

Soft-Sector (Buffered Stepping, Polling Disabled). In this mode, the appropriate number of high-speed stepping pulses are sent as soon as the Seek command is issued. If the drive enters a not-ready state, or if SKC (seek complete) is not asserted within the time it takes to send the required number of pulses in normal stepping mode, then the Seek command is terminated normally (generating an interrupt). The IST byte is available as a result byte and the appropriate bit is set; i.e., SER and EQC or NR (not ready). If the seek operation is successful, the Seek command is terminated normally (CEH = 1) and the SEN bit of the IST byte is set. The IST byte is available as a result byte. The Sense Interrupt Status command is not allowed (SRQ is not set), nor can seek operations be overlapped in this mode.

Format

0111S	PHN	(PSN)	SCNT	DPAT	GPL1	(GPL3)	
	EST	SCNT					

PHN = Physical Head Number
PSN = Physical Sector Number
SCNT = Sector Count
DPAT = Data Pattern
GPL1 = Gap Length 1
GPL3 = Gap Length 3
EST = Error Status

This command is used to write the desired ID and data format on the disk.

(1) When using hard-sector drives, this command will begin format-writing at the sector specified by PHN and PSN, which are loaded during command phase.

When soft-sector drives are specified, this command will begin format-writing at the sector immediately following the index pulse on the track specified by PHN.

In either case, data transmitted from the local memory by DMA operation is written into the ID field, and the data field is filled with the data constant specified by DPAT until DTL (data length) is zero. DTL is established during the specify command with DTLH and DTTL. The sector count, SCNT, is decremented by one at the end of the Format operation on each sector. The following bytes are required by the HDC for each sector: (FLAG), LCNH, LCNL, LHN, and LSN. FLAG is omitted on soft-sector drives. These bytes are transferred by DMA.

The format operation produces the various gaps with length as specified by GPL1, GPL2 (See Specify), and GPL3 (For soft-sector only.)

Note:
GPL3 may not exceed decimal value of 44.

(2) The above operation is repeated until SCNT is equal to zero. The execution of the command is terminated normally, when the content of SCNT is equal to zero and the second index pulse has occurred.

(3) When using a hard-sector drive, it is possible to write the ID field displaced from the normal position by 64 bytes by setting the skew bit of the command byte ((S) = 1). This is useful when defective media prevent writing in the normal area of the sector.

(4) Items 4, 5, and 8 of the Read Data and item 4 of the Write Data command are identical for this command. Refer to these items (which appear later in this section) for remaining format operation details.

Verify ID

1000S	PHN	(PSN)	SCNT	
	EST	SCNT		

PHN = Physical Head Number
PSN = Physical Sector Number
SCNT = Sector Count
EST = Error Status

ID bytes of specified sectors are read and compared with the data that are accessed from local memory via DMA control. The first sector that is verified is specified by PHN and PSN when a hard-sector disk is used. For soft-sector disks, only PHN is given and the Verify ID command begins comparisons with the first physical sector on the track.

Byte comparisons continue as long as successful or until the sector count is zero or a CRC error is found.

When using a hard-sector drive, it is possible to have the HDC verify a skewed ID field by setting the skew bit of the command byte. Refer to the Format section, given earlier, for details.

Read ID

1001S	PHN	PSN	SCNT	
	EST	SCNT		

PHN = Physical Head Number
PSN = Physical Sector Number
SCNT = Sector Count
EST = Error Status

ID bytes of specified sectors are read and transferred to local memory by DMA.

Hard-sector disks: Beginning with the sector specified by PHN and PSN, the ID bytes of each sector (FLAG, LCNH, LCNL, LHN, LSN) are read until an error is found or the SCNT has reached zero.

It is also possible to perform the above operation with skewed ID fields by setting the skew bit of the command byte. This will allow reading ID fields that have been shifted by 64 bytes by the Skewed Format command.

Soft-sector disks: This command will begin checking ID fields immediately following the index pulse and will continue until one valid ID field is read, or until the second index pulse is detected or SCNT = 0, whichever occurs first. Four bytes per soft sector are read: LCNH, LCNL, LHN, and LSN.

Read Diagnostic

1010X	PHN	PSN	
	EST		

PHN = Physical Head Number
PSN = Physical Sector Number
EST = Error Status

This command is implemented only for hard-sector disks. The desired physical sector is specified, and the data field will be read even if the ID bytes of that sector contain a CRC error. Only one sector at a time may be read by this command.

Read Data

1011X	PHN	(FLAG)	LCNH	LCNL	LHN	LSN	SCNT
	EST	PHN	(FLAG)	LCNH	LCNL	LHN	LSN	SCNT

PHN = Physical Head Number
FLAG = Flag Byte, Hard-Sector ID Field Only
LCNH = Logical Cylinder Number, High Byte
LCNL = Logical Cylinder Number, Low Byte
LHN = Logical Head Number
LSN = Logical Sector Number
SCNT = Sector Number
EST = Error Status

This command is used to read and transfer data via DMA from the disk to the local memory.

(1) The HDC reads data from the specified sector which is determined by the following preset parameters: FLAG (for hard-sector only), LCNH, LCNL, LHN, and LSN. The drive is selected by UA (unit address) in the command byte. The HDC then transfers the read data to the local memory via DMA operation.

(2) After reading each sector, the HDC updates the SCNT and LSN to point to the next sector, and repeats the above described operation until SCNT is equal to zero. During the above read operations, if LSN is equal to ESN, the HDC updates LSN, and continues the read operations after relocating the head (track) specified by LHN.

(3) The HDC abnormally terminates the execution of this command if SCNT is not equal to zero when the HDC reads out the data from the last sector (LSN = ESN and LHN = ETN). The ENC (end of cylinder) bit of EST (error status) is set to one in this situation.

(4) The HDC will terminate this command if a fault signal is detected while reading data. The HDC will set the EQC (equipment check) of the EST (error status) byte when this occurs.

(5) The HDC will terminate this command abnormally if the ready signal from the drive is not active or becomes not active while a Read Data command is being performed. The NR (not ready) bit of the EST (error status) register will be set to one in this case.

(6) The HDC will end this command abnormally if it cannot find an AM (address mark) (soft-sector mode) or a SYNC byte (hard-sector mode) of the ID field before four index pulses occur. Under these conditions, the RRQ (reset request) bit of the STR (status register) will be set. In order to perform further disk commands the HDC will have to be reset because the format controller is hung up looking for an AM or SYNC byte.

(7) ECC mode: If the HDC detects an ECC error during a read operation, it will execute the following operations: First, the HDC decides whether or not the error is correctable by checking the syndrome of the error pattern. If the error is correctable, the HDC terminates the command in the normal mode after setting the DER (data error) bit of EST register to one. The host system can input the error address and the error pattern information by issuing the Detect Error command. If it is not a correctable error, the HDC will terminate the command in the abnormal mode after setting the DER bit of the EST register to one.

CRC mode: If the HDC detects a CRC error on a sector during the read operation, the HDC will terminate the command in the abnormal mode after setting the DER bit of the EST register to one.

(8) If the HDC detects an overrun condition during a Read Data operation, the OVR (overrun) bit of the EST register is set. (An overrun condition occurs when the internal data FIFO is full, another data byte has been received from the disk drive, and a DMA service does not occur.) The command is then terminated in the abnormal mode.

(9) If the HDC cannot find the desired sector within the occurrence of three index pulses, the ND (no data) bit of the EST register is set to one and the command is terminated in the abnormal mode.

(10) If TC (terminal count) occurs during a Read Data command the DMA transfers to the local memory will stop. However, the HDC does continue the read operation until the end of the sector, if SCNT = 1.

If SCNT is 2 or more, DMA transfers restart when SCNT is updated to the next sector, and will continue until SCNT is zero.

(11) If the Read Data command has been successfully completed, the result status will be set indicating such, and the result status bytes will be updated according to the number of sectors that have been read. The logical disk parameters—LSN, LHN, and LCN—are incremented as follows:

LSN is incremented at the end of each sector until the value of ESN is reached. LSN is then set to 0 and LHN is incremented. If LHN reaches the value of ETN, then LHN is cleared and LCN is incremented.

In other words, if a Read or Write operation is terminated normally, the various parameters will point to the next logical sector.

If the command is terminated in the abnormal mode, the result status bytes will indicate on which sector, cylinder, and head the error occurred.

(12) If the HDC cannot detect the address mark (soft-sector) or SYNC bytes (hard-sector) immediately following the VFO sync in the data field, the HDC will set the MAM (missing address mark) bit of the EST register to one, and will terminate the command in the abnormal mode.

Check

1100X	PHN	(FLAG)	LCNH	LCNL	LHN	LSN	SCNT	
	EST	PHN	(FLAG)	LCNH	LCNL	LHN	LSN	SCNT

PHN = Physical Head Number
FLAG = Flag Byte, Hard-Sector ID Field Only
LCNH = Logical Cylinder Number, High Byte
LCNL = Logical Cylinder Number, Low Byte
LHN = Logical Head Number
LSN = Logical Sector Number
SCNT = Sector Number
EST = Error Status

This command is used to confirm that the data previously written to the medium by the Write Data command contains the correct CRC or ECC.

(1) The HDC reads the data in the sector specified by FLAG (hard-sector only), LCNH, LCNL, LHN, and LSN. The Check command differs from the Read Data command in that no DMA transfers occur.

With the exception of the ECC mode, the Check command is the same as the Read Data command. Please refer to items 2, 3, 4, 5, 6, 7, 8, 11, and 12 of Read Data command for details.

(2) If in the ECC mode, the HDC detects only ECC errors and does not execute any error correction operation even if the ECC errors are correctable. No data transfers have been made, and there is no data to correct.

Scan

1101X	PHN	(FLAG)	LCNH	LCNL	LHN	LSN	SCNT	
	EST	PHN	(FLAG)	LCNH	LCNL	LHN	LSN	SCNT

PHN = Physical Head Number
FLAG = Flag Byte, Hard-Sector ID Field Only
LCNH = Logical Cylinder Number, High Byte
LCNL = Logical Cylinder Number, Low Byte
LHN = Logical Head Number
LSN = Logical Sector Number
SCNT = Sector Number
EST = Error Status

(1) In executing the Scan command, the HDC reads the data from the sector specified by the preset parameters of the command phase. The HDC then compares this data with the data transmitted from the local memory. (The purpose of this command is to locate a sector that contains the same data as the local memory.)

This command will terminate successfully if the data from the disk and the data from the local memory are the same. If they are not, the HDC updates SCNT and LSN, and executes the abovementioned operation again.

If the HDC cannot locate a sector that satisfies the scan conditions, the NCI bit of the STR will be set. The HDC tries to compare data until the end of the cylinder has been reached, or until SCNT is zero.

(2) If the value of the LSN (logical sector number) is equal to that of ESN (ending sector number) after updating LSN, the HDC updates the contents of LHN (increasing by 1) and that of LSN (LSN = 0), and repeats the operation described in item 1 after selecting the next head.

(3) After comparing the data transferred from the host CPU with the data in the specified sectors, the result bytes (FLAG, which is only for hard-sector disks, LCNH, LCNL, LHN, and LSN) will be set equal to the sector location that satisfies the Scan command.

(4) The descriptions in 4, 5, 6, 8, and 9 of Read Data command, and items 3 and 4 of Verify Data command are identical for this command. Refer to these descriptions for additional details.

Verify Data

1110X	PHN	(FLAG)	LCNH	LCNL	LHN	LSN	SCNT	
	EST	PHN	(FLAG)	LCNH	LCNL	LHN	LSN	SCNT

PHN = Physical Head Number
FLAG = Flag Byte, Hard-Sector ID Field Only
LCNH = Logical Cylinder Number, High Byte
LCNL = Logical Cylinder Number, Low Byte
LHN = Logical Head Number
LSN = Logical Sector Number
SCNT = Sector Number
EST = Error Status

This command is used to verify data on the disk.

(1) The HDC reads the data from the specified sector, and compares the data transmitted from the local memory via DMA with the data from the disk.

The sector is specified by FLAG (hard-sector only), LCNH, LCNL, LHN, and LSN, and the drive is selected by UA. If the data transmitted from the local memory is the same as that read from the sector, the HDC updates the contents of LSN and SCNT, and continues the abovementioned operation. After updating SCNT, if the value of SCNT is equal to zero, the HDC ends the execution of the command in the normal mode. If the value of LSN is equal to that of ESN after updating LSN, the HDC updates the contents of LHN and LSN, and the HDC continues the verify data operation after selecting the head (track) specified by LHN.

If the data transmitted from the local memory is not the same as that read from the sector, the HDC ends the execution of the command in the abnormal mode after setting the NCI (not coincident) bit of STR to one.

(2) If, after verifying the data on the last sector, the contents of SCNT are not equal to zero, the HDC terminates execution of the command abnormally after setting the ENC (end of cylinder) bit of the EST register to one.

(3) After verifying the data read from a sector, the HDC checks the CRC bytes (CRC mode) or the ECC bytes (ECC mode).

If the HDC detects a CRC or an ECC error on a sector, the HDC terminates execution of the command abnormally after setting the DER bit of the EST register to a one.

(4) After detecting an active $\overline{TC}$ signal ($\overline{TC} = 0$), the HDC executes the above operation by comparing the read data from the disk drive with the data 00 instead of the data from the main system until the end of the sector.

In the case of SCNT greater than one, when SCNT is updated, DMA transfers restart and disk data is compared against host data until SCNT is zero.

(5) After verification of the data on all the sectors, FLAG (hard-sector only), LCNH, LCNL, LHN, and LSN are set to the values of FLAG, LCNH, LCNL, LHN, and LSN of the last verified sector.

(6) The descriptions in items 4, 5, 6, 8, 9, and 12 of the Read Data command are valid in this command. Please refer to these items for additional detail.

Write Data

1111X	PHN	(FLAG)	LCNH	LCNL	LHN	LSN	SCNT	
	EST	PHN	(FLAG)	LCNH	LCNL	LHN	LSN	SCNT

PHN = Physical Head Number
FLAG = Flag Byte, Hard-Sector ID Field Only
LCNH = Logical Cylinder Number, High Byte
LCNL = Logical Cylinder Number, Low Byte
LHN = Logical Head Number
LSN = Logical Sector Number
SCNT = Sector Number
EST = Error Status

(1) This command is used to write data into the data field of the sectors specifed by FLAG (hard disks only), LCNH, LCNL, LHN, and LSN, and to write CRC bytes or ECC bytes according to each internally specified mode (CRC or ECC). The data is written to the disk via DMA transfer from the local memory.

(2) After writing data on a sector, the HDC updates the contents of SCNT and LSN, and repeats the above described Write Data operation until SCNT is equal to zero.

During the above Write Data operations, if LSN is equal to ESN, the HDC updates LHN and LSN, and continues the Write Data operations after selecting the new head (track) specified by LHN.

As described above, the HDC has the capability of multi-sector and multi-track write operations.

(3) The HDC abnormally terminates the execution of this command if the SCNT is not equal to zero when the HDC writes the data to the last sector (LSN = ESN and LHN = ETN). The ENC (end of cylinder) bit of EST (error status) register is set to one in this situation.

(4) If the write protected signal is active (high) at the beginning of the execution of this command, the HDC ends the execution of this command in the abnormal mode after setting the NWR (not writable) bit of the EST register to one.

(5) After detecting an active $\overline{TC}$ signal ($\overline{TC} = 0$), the HDC writes the data 00 to the sector, instead of the data from the host system.

In the case of SCNT of two or more, when SCNT is updated, the DMA transfers will restart and writing of host data will continue until SCNT = 0.

(6) In the ST506-type mode, the HDC will set the reduced write current output bit to a one when the cylinder number becomes greater than that specified by RWCH and RWCL. These parameters are loaded during execution of the Specify command.

The descriptions in items 4, 5, 6, 8, 9, and 11 of the Read Data command are applicable here also. Refer to these items for further detail.

Sense Interrupt Status

0001X	
	IST

IST = Interrupt Status

(1) The HDC transfers the new disk status to the host CPU at the end of a Seek or Recalibrate operation or the new disk status resulting from a change of state of the ready signal, which may occur at any time.

(2) If the Seek or Recalibrate command in progress is completed when this command is issued or if there has been no change of state of the ready signal from the drive, this command will be terminated abnormally.

Specify

0010X	MODE	DTLH	DTLL	ETN	ESN	GPL2	(MGPL1) [RWCH]	[RWCL]

MODE = Mode Byte; Selects Operation Mode
DTLH = Data Length, High Byte
DTLL = Data Length, Low Byte
ETN = Ending Track Number
ESN = Ending Sector Number
GPL2 = Gap Length 2
MGPL1 = Gap Length 1 (used in SMD mode only); Controls Read Gate Timing
RWCH = Reduced Write Current (Cylinder No.), High Byte
RWCL = Reduced Write Current (Cylinder No.), Low Byte

The Specify command is used to set the operational mode of the HDC by presetting various parameters. Parameters such as MODE (figure 5, table 7), DTLH (figure 6), DTLL, ETN, ESN, GPL2, MGPL1/RWCH, and RWCL may be programmed into the HDC. This allows for a high degree of versatility. Data record length is programmable from 128 to 4095 bytes in soft-sector mode and 256 to 4095 bytes in hard-sector mode.

Figure 5. Mode Byte

0	ECC	CRCS	SSEC	DSL/ STP3	DSE/ STP2	SOM/ STP1	SOP/ STP0

Figure 6. DTLH Byte

1	CRC·	PAD	POL	DTL11	DTL10	DTL9	DTL8

CRC· = Initial Value of Polynomial Counter, Either All Zeros or All Ones
PAD = Selects ID/Data pad of 00H if 0
= Selects ID/Data pad of 4EH if 1
POL = Polling Mode if 0
= Nonpolling Mode if 1

Table 7. Mode Byte Bits

Bit Name	Specified Mode		
ECC	1 ECC is appended in data field: $(x^{21}+1)(x^{11}+x^2+1)$		
	0 CRC is appended in data field		
CRCS	1 Generator polynomial: $(x^{16}+1)$		
	0 Generator polynomial: $(x^{16}+x^{12}+x^5+1)$		
SSEC	1 Soft-sector disk (floppy-like interface), MFM data		
	0 Hard-sector disk (SMD interface), NRZ data		
	SSEC = 0		**SSEC = 1**
DSL	Data strobe late	STP3	(Note 1)
DSE	Data strobe early	STP2	(Note 1)
SOM	Servo offset minus	STP1	(Note 1)
SOP	Servo offset plus	STP0	(Note 1)

Note:
(1) Stepping rate for ST506 mode = (16-STP) × 2110 × t_{CY}
Assuming a 10 MHz processor clock: F_H = 2.11 ms...O_H = 33.76 ms

Sense Unit Status

Soft-Sector Mode

0011X	
	UST

SMD Mode

0011X	1	2	5
	UST	DS	DT

The Sense Unit Status (SUS) command is used to transfer the Unit Status (UST) to the host. In the case of SMD mode the SUS command may also be used to transfer the Detail Status (DS) and Device Type (DT) by using the appropriate preset parameter value as shown above. No preset parameters are used in the soft-sector mode, although one is required in the SMD mode. Values other than 1, 2, or 5 do not produce valid results.

After result bytes are placed in FIFO, HDC generates a FAULT CLEAR when in SMD mode.

The DS and DT bytes are defined by the type of drives used. The UST is shown in table 8.

Table 8. Unit Status Byte

Bit No.	Interface Type: SMD	Interface Type: ST506
D_7	Unit selected	0
D_6	Seek end	0
D_5	Write protected	0
D_4	0	Drive selected
D_3	Unit ready	Seek complete
D_2	On cylinder	Track 000
D_1	Seek error	Ready
D_0	Fault	Write fault

Detect Error

0100X	
	EADH EADL EPT1 EPT2 EPT3

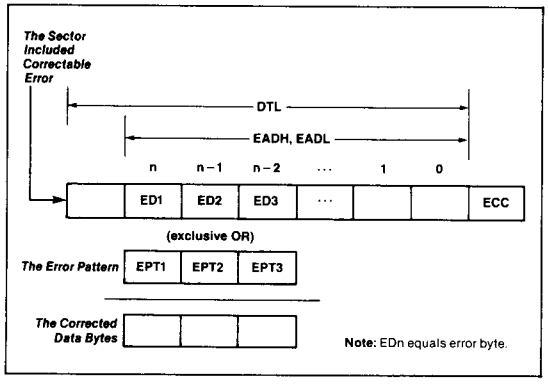
EADH = Error Address, High Byte
EADL = Error Address, Low Byte
EPT1 = Error Pattern, Byte 1
EPT2 = Error Pattern, Byte 2
EPT3 = Error Pattern, Byte 3

This command is used to transfer the error pattern and the error address to the host CPU, when correctable errors have occurred during the execution of a Read Data command with the ECC mode enabled.

The error address (EADH and EADL) is calculated from the last data byte of the sector that contained a correctable error which was indicated by the status bit of the previous Read Data command with the ECC mode enabled. The error pattern is used for correcting the error data at the location where the error occurred. After receiving the error address and the error pattern, the host CPU can correct the error data by performing an exclusive-OR of the error pattern and the error data. See figure 7.

The result bytes are available to the host CPU within 100μs.

Figure 7. Error Correction



Auxiliary Command

0000AAAA	

There are no preset parameters or result bytes associated with this command. The definitions of the 4 LSBs (AAAA) are given in figure 8 and table 9. The auxiliary command is accepted at any time and is immediately executed. The auxiliary command may be used to recover from certain types of error conditions, or to mask and clear interrupts.

Figure 8. Auxiliary Command

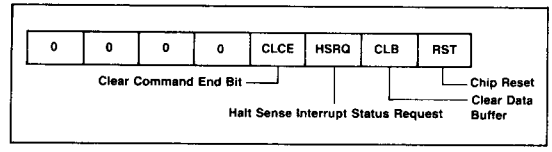


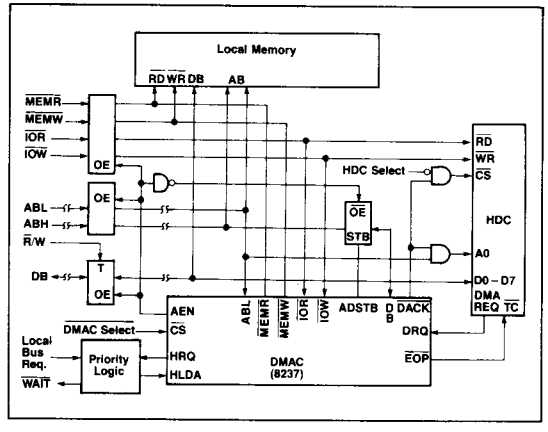
Table 9. Auxiliary Command Bits

Bit Name	Operation
CLCE	Clears the CE bits of the status register, inactivating the interrupt request output caused by Command End condition. This is used when no disk commands are going to be issued and it is desired to clear the interrupt.
HSRQ	Deactivates the interrupt request output caused by Sense Interrupt Status Request condition until a Command End occurs. However, this command has no effect on the SRQ bit of the status register.
CLB	Clears the data buffer.
RST	This has the same effect as a reset signal on the Reset input. This function is used whenever the RRQ bit in the status register is set (indicating the format controller is hung up), or when a software reset is needed.

System Example

Figure 9 shows an example of a local bus system.

Figure 9. Local Bus System



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Track Format

Figure 10 shows track format for hard- and soft-sectored disks.

System Example Timing Diagrams

Figures 11 through 22 show the interface timing (soft-sector and hard-sector) required to interface the hard disk drive.

Figure 10. Track Format

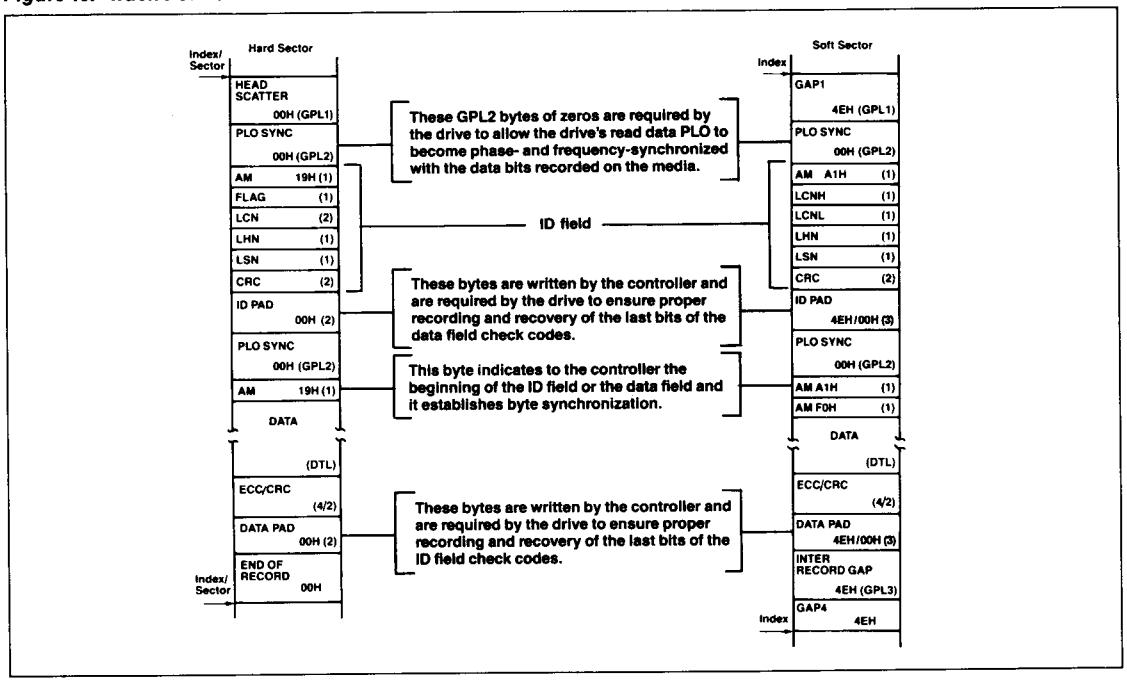
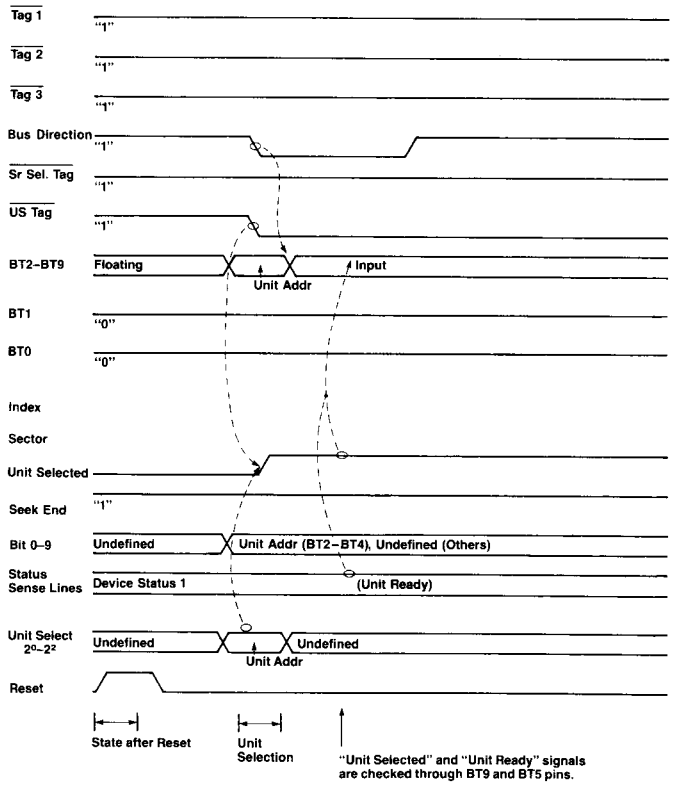


Figure 11. "Unit Selection" and "State Sense" Timing (Hard Sector)



83-003499B

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Figure 12. Return to Zero Timing (Hard Sector)

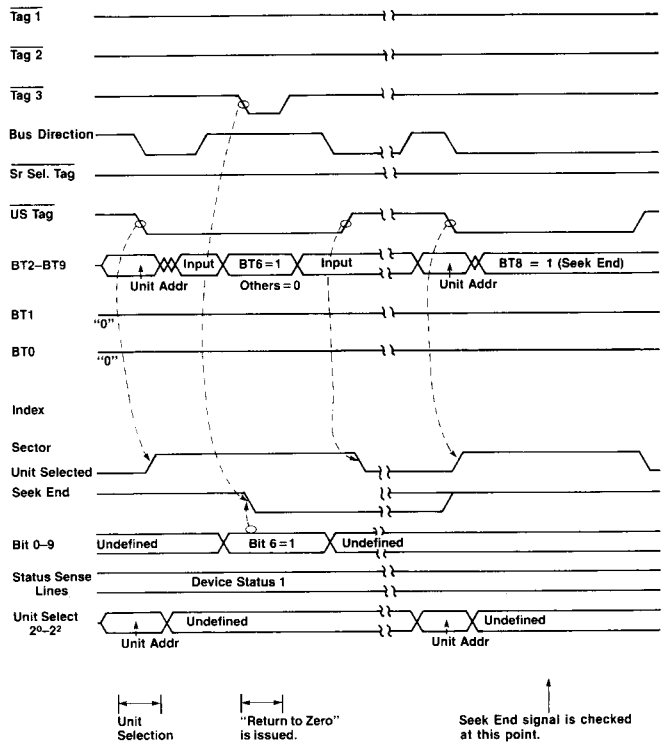

Figure 13. "Seek" Timing (Hard Sector)

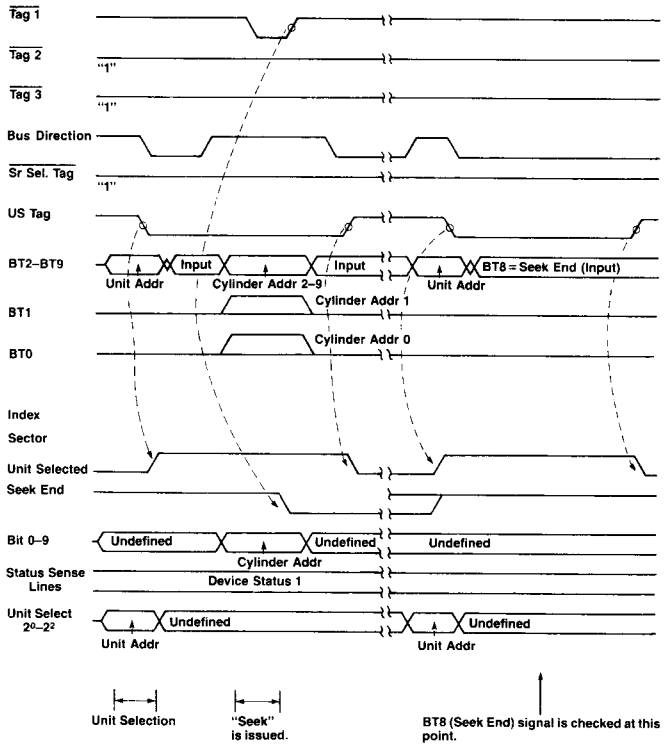

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Figure 14. "Head Select" Timing (Hard Sector)

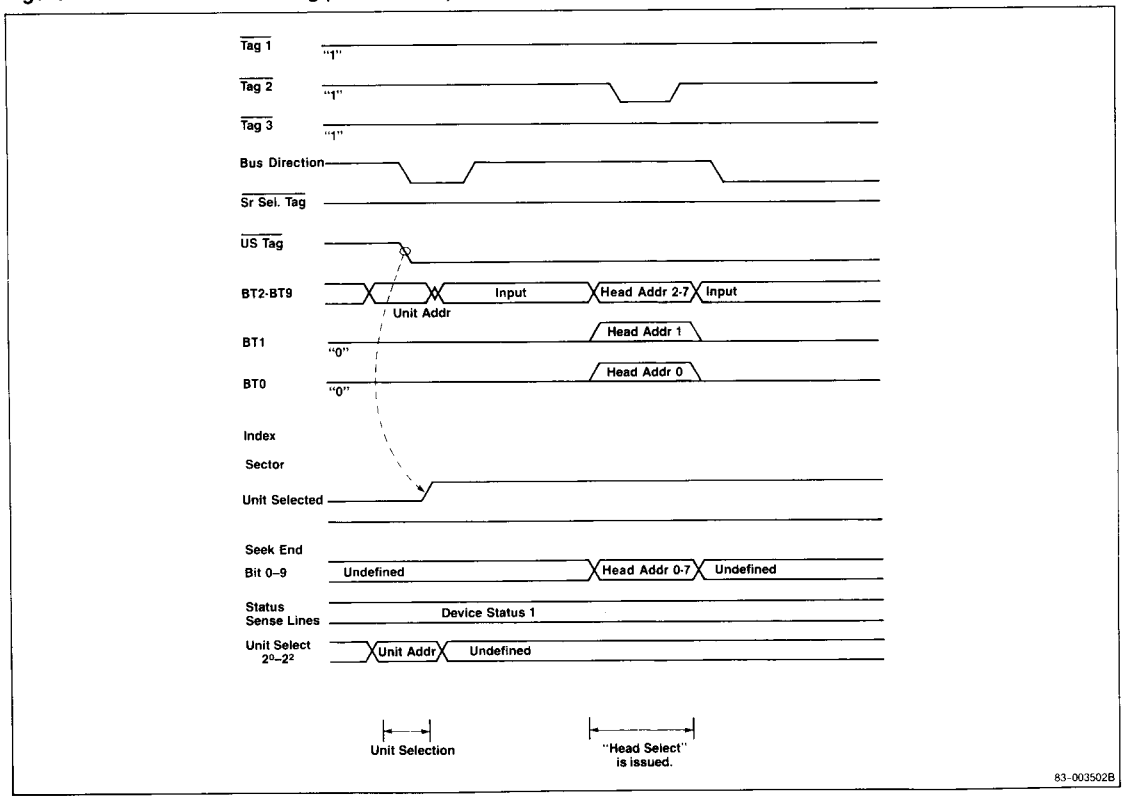

Figure 15. "Unit Status Sense' Timing (Hard Sector)

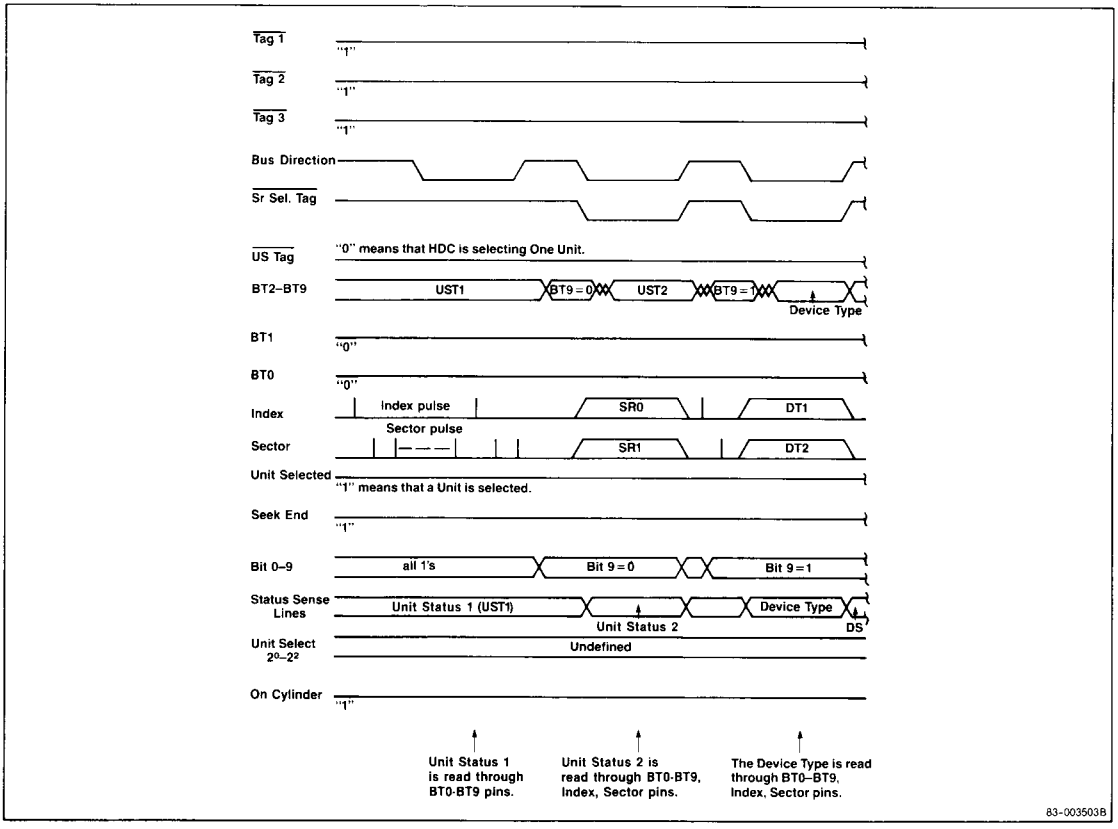

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Figure 16. "Data Read" Timing (Hard Sector)

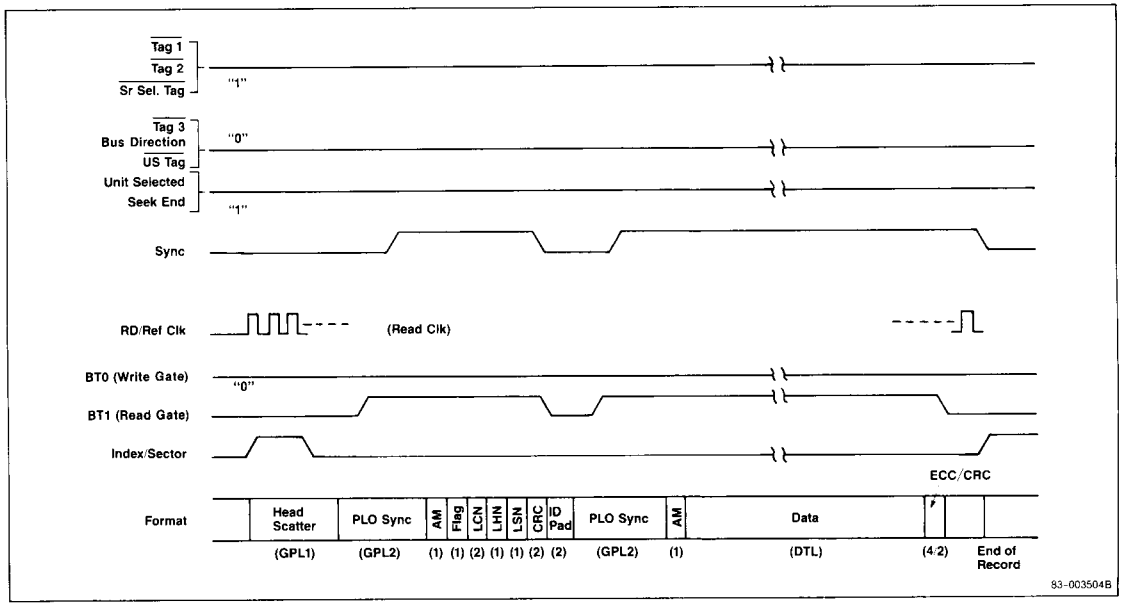

Figure 17. "Data Write" Timing (Hard Sector)

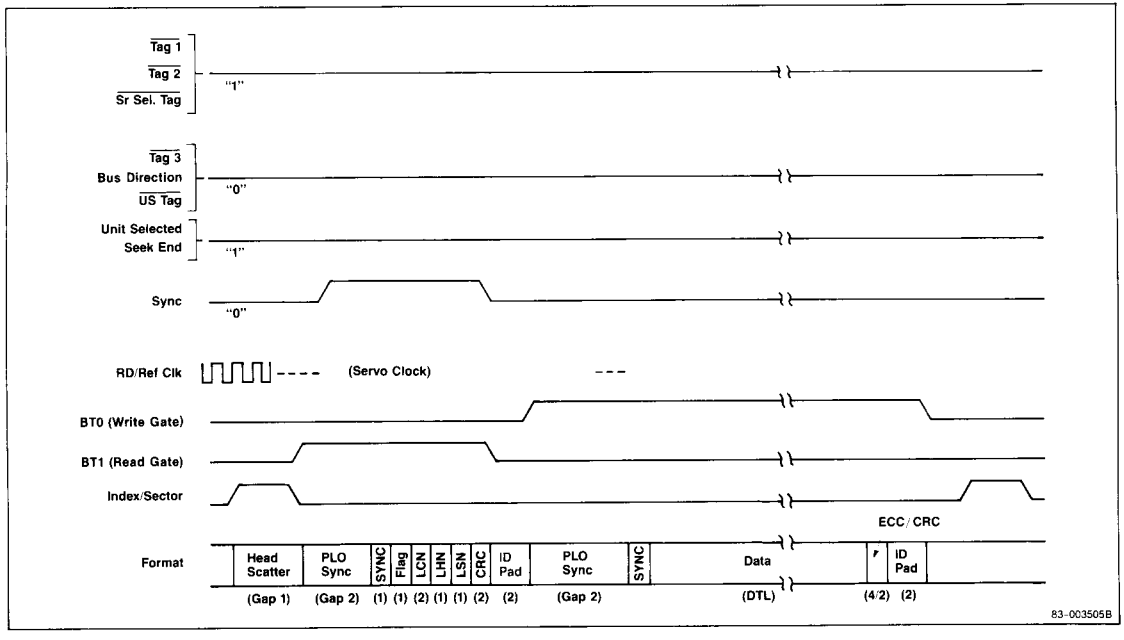

Figure 18. "Drive Select" and "Unit Status Sense" Timing (Soft Sector)

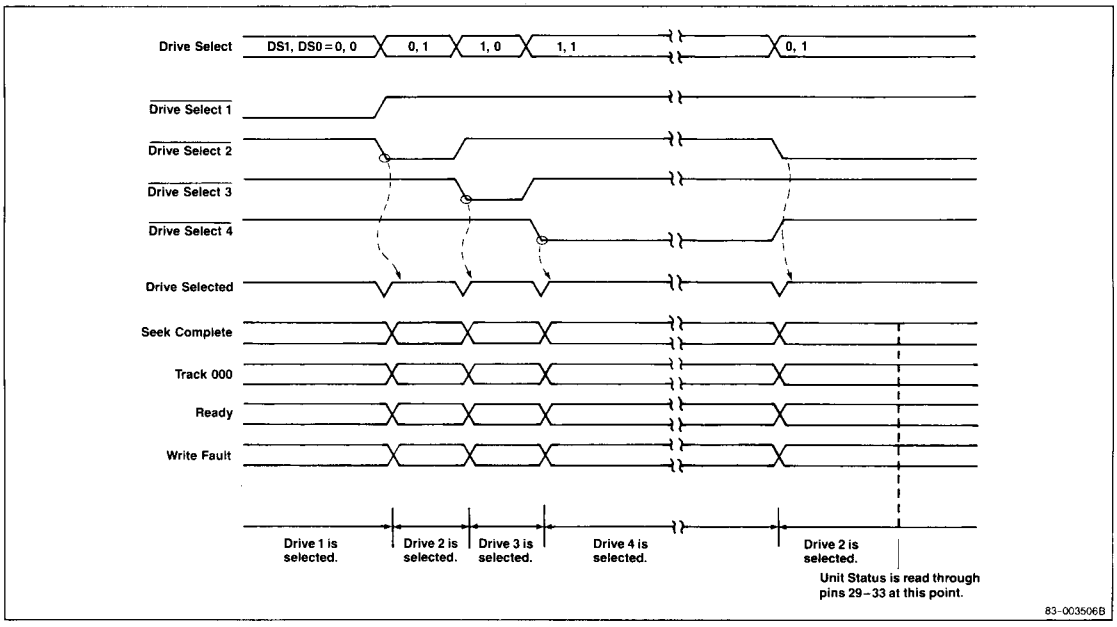

Figure 19. "Normal Seek" Timing (Soft Sector)

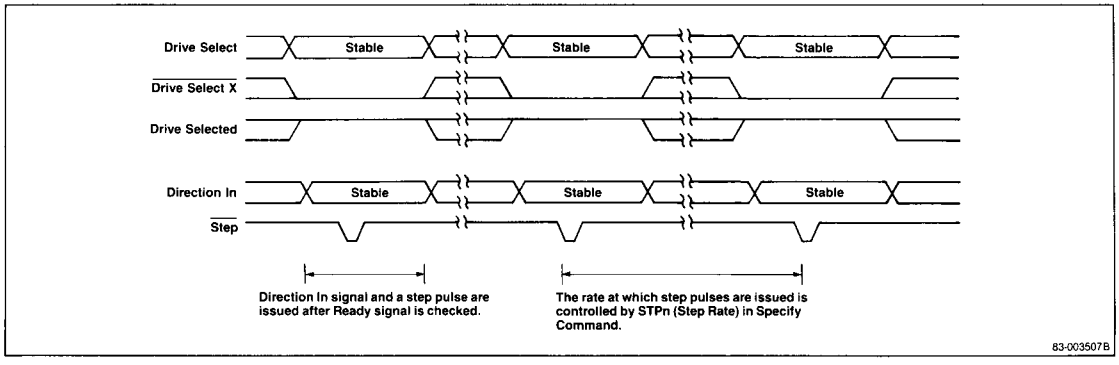

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Figure 20. "Buffered Seek" Timing (Soft Sector)

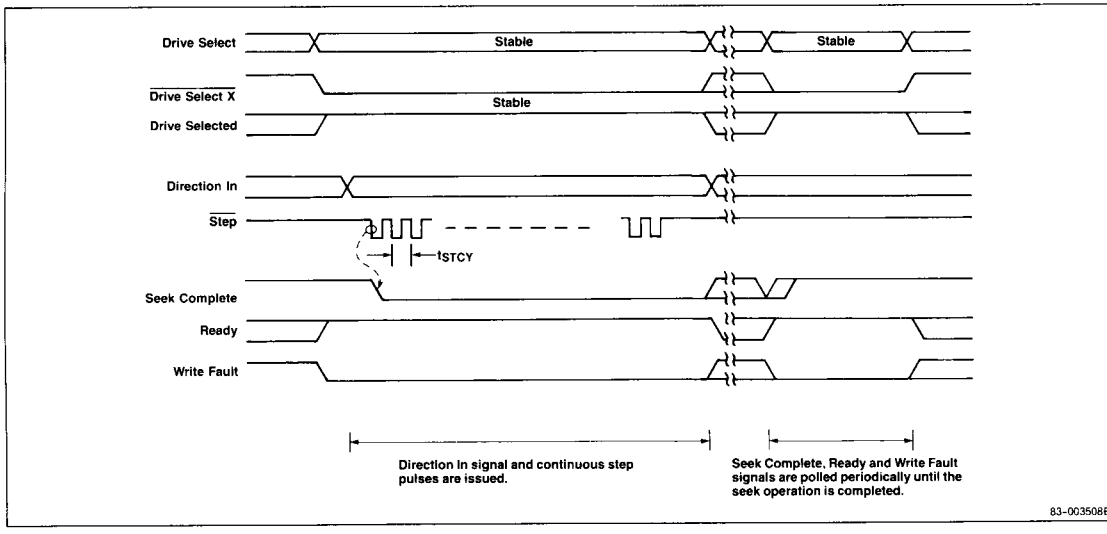


Figure 21. "Data Read" Timing (Soft Sector)

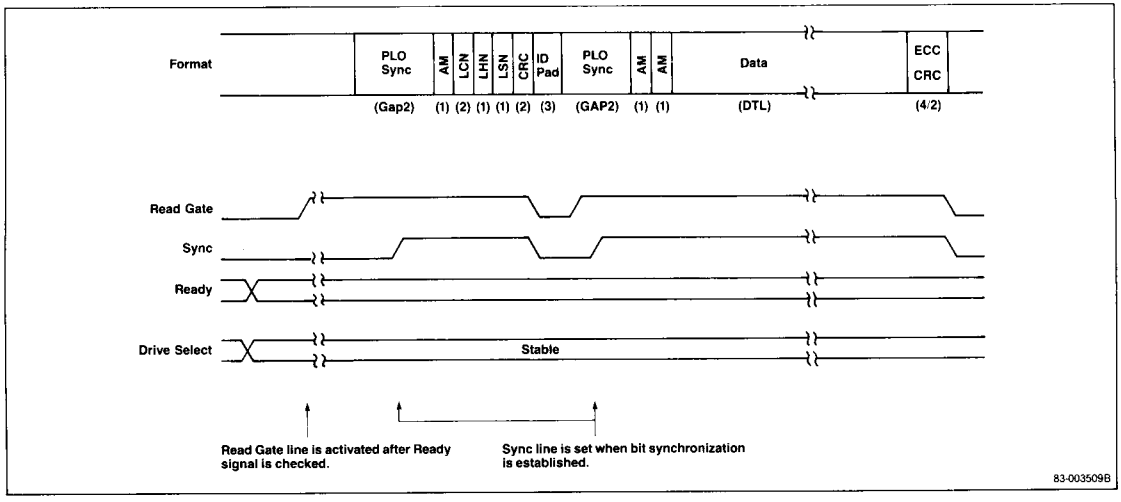
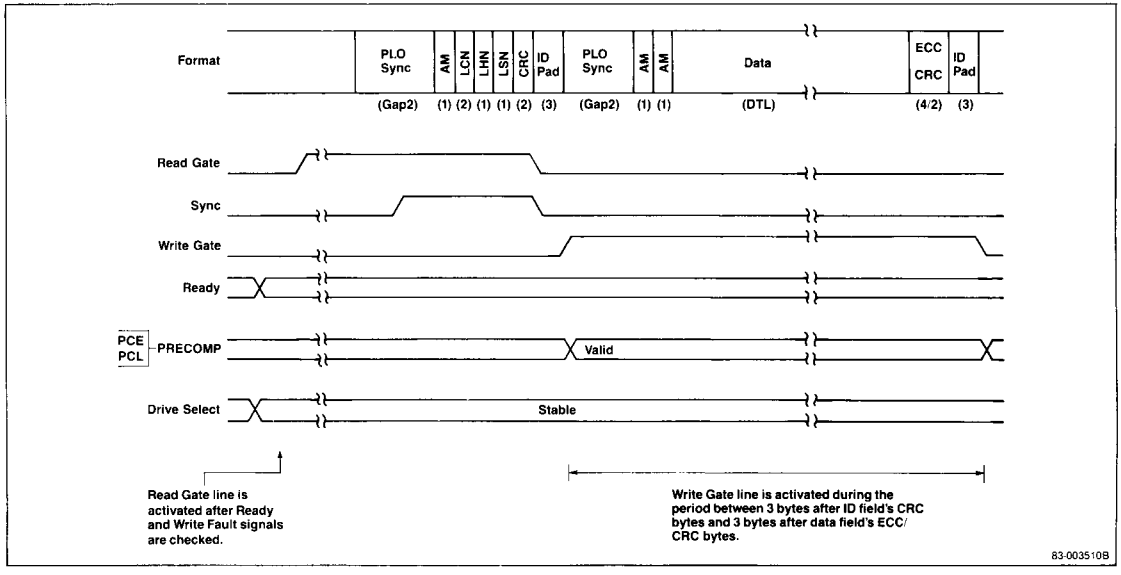


Figure 22. "Data Write" Timing (Soft Sector)



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